

HotSpot Extension 1.2 Test Cases

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Computing Joint Parallel Resistivity

$$\begin{aligned}\text{Let } A_{\%w/oTSVs} &= \% \text{ area of block without TSVs} \\ A_{\%withTSVs} &= \% \text{ area of block with TSVs} \\ R_{Layer} &= \text{Resistivity of the Layer (TIM or Silicon)} \\ R_{Cu} &= \text{Resistivity of TSVs (Copper)} = 0.0025 \frac{m \cdot K}{w} \\ R_{Joint} &= \frac{1}{\left(A_{\%w/oTSVs} * \frac{1}{R_{Layer}} \right) + \left(A_{\%withTSVs} * \frac{1}{R_{Cu}} \right)}\end{aligned}$$

In order to calculate the percent area of block with TSVs you can model the TSVs with diameter $50\mu m^1$ as square blocks, i.e. occupying a space of $50\mu m \times 50\mu m$. Smaller TSVs dimensions are also possible in current technologies, such as $10\mu m \times 10\mu m$. You should also consider the minimum pitch requirements in between the TSVs in your design.

Test Case Parameters

Sampling Interval	=	0.0001 seconds
# of Row	=	64
# of Cols	=	64
Resistivity of Silicon	=	$0.01 \frac{m \cdot K}{w}$
Resistivity of Interface Material	=	$0.25 \frac{m \cdot K}{w}$
Length/Width of one layer	=	2mm x 2mm

Other parameters are listed in the HotSpot Configuration File/Layer Configuration File

¹ Mohamed M. Sabry, Ayse K. Coskun, David Atienza, Tajana Simunic Rosing, Thomas Brunschweiler. **Energy- efficient Multi-objective Thermal Control for Liquid-Cooled 3D Stacked Architectures**. In *IEEE Transactions on Computer Aided Design*, vol. 30 no. 12, pp. 1883-1896, Dec. 2011.

Default3D

Base case with one unit in each layer and default parameters.

Layer #	Floorplan File	Resistivity $\left(\frac{m \cdot K}{W}\right)$
0	layer0.flp	0.01
1	TIM.flp	0.25
2	layer2.flp	0.01
3	TIM.flp	0.25

3D_10Percent

This test case consists of four layers with each containing only one unit in each layer. The 3D_10percent_TIM.flp layer has a TSV density of ten percent and the joint resistivity is calculated based on the equation in the above section.

Layer #	Floorplan File	Resistivity $\left(\frac{m \cdot K}{W}\right)$
0	layer0.flp	0.01
1	10percent_TIM.flp	0.02294
2	layer2.flp	0.01
3	TIM.flp	0.25

3D_2Percent

This test case consists of four layers with each containing only one unit in each layer. The 3D_2percent_TIM.flp layer has a TSVs density of two percent.

Layer #	Floorplan File	Resistivity $\left(\frac{m*K}{w}\right)$
0	layer0.flp	0.01
1	2percent_TIM.flp	0.08389
2	layer2.flp	0.01
3	TIM.flp	0.25

3D_2Percent_v2

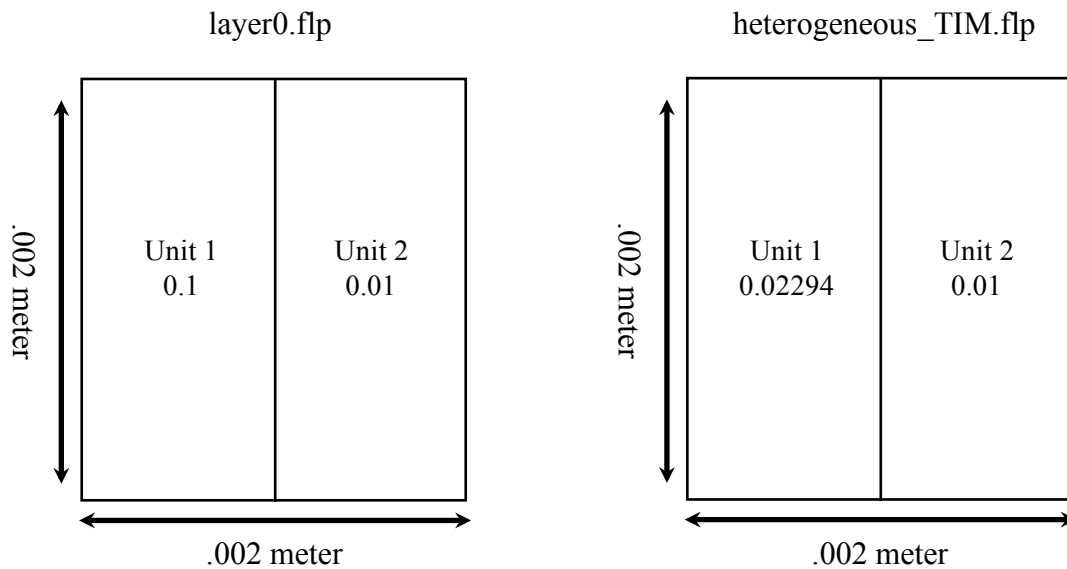
TSVs may connect the active transistor layers of each Si chip, therefore some of the Si chips may have TSVs in the bulk Si. We adjusted the resistivity in layer zero to model this case with the same two percent TSVs density.

Layer #	Floorplan File	Resistivity $\left(\frac{m*K}{w}\right)$
0	2percent_layer0.flp	0.0094
1	2percent_TIM.flp	0.02294
2	layer2.flp	0.01
3	TIM.flp	0.25

3D_heterogenous

The first layer of Silicon consists of two evenly sized blocks with equal thermal resistivity values. The first layer of TIM consists of two evenly sized blocks: one with default thermal resistivity value, and the other with a modified thermal resistivity value. Other layers are unchanged.

Layer #	Floorplan File	Resistivity $\left(\frac{m \cdot K}{W}\right)$
0	layer0.flp	Unit1 = 0.01
		Unit2 = 0.01
1	heterogeneous_TIM.flp	Unit1 = 0.02294
		Unit2 = 0.01
2	layer2.flp	0.01
3	TIM.flp	0.25



Note: We do not modify the specific heat capacity of the layer in these experiments. The change in specific heat capacity is expected to have lower impact compared to that of the thermal resistivity. Specific heat capacity values, however, can also be modified by editing the floorplan file.

Debugging

We added a debugging flag to print out the thermal resistances in the x, y and z direction for each grid in a .csv type format. This will disable the dumping of steady state temperatures to stdout.

Usage:

```
make DEBUG3D=1
```

When running HotSpot it outputs the relevant data starting from layer zero to the last layer specified in the layer configuration file.

Output:

```
row #, column #, Rx, Ry, Rz
```