ENG EC571 - Digital VLSI Circuit Design

Term: Spring 2025

Lectures: Mon-Wed 12:20 – 2:05 pm in CDS 262

Recitation/Lab Sessions: Friday 2:30 – 4:15 pm in PHO 305

Please apply for the PHO 305 and PHO 307 room access online through the Access Management Portal by Friday – January 24th, 12:00pm.

Number of Credits: 4

Pre-requisites: EC 311 and EC 410 or equivalents are pre-requisites for this course.
Please talk to us if you have any questions about pre-requisites.

Course Objectives
By the end of the course, students should be able to:

- Design a digital CMOS circuit that performs some arbitrary logical function to a given area, power, and performance metric.
- Build an intuition for tradeoffs between these performance metrics and iterate on the design to optimize them.

Staff Information

Instructor:

Name:	Rabia Yazicigil Kirby
Office address:	PHO 329
Office phone number:	617-353-2815
E-mail address:	rty@bu.edu – Include EC 571 in the subject line
Office hours:	PHO 329, Monday 3:30 pm to 4:30 pm or by appointment

Lab Assistant/Grader:

Name:	Zeynep Ece Kizilates
E-mail address:	zecek@bu.edu – Include EC 571 in the subject line
Office hours:	PHO 305, Tuesday and Thursday 5:30 pm to 6:30 pm or by appointment

Course Learning Goals:
By taking this course, students should be able to:

(1) Understand the MOSFET basics and their fabrication and the layout design rules.
(2) Understand the operation of MOS transistor.
(3) Understand the static characteristics of MOS inverters.
(4) Design, implement and simulate: Inverter Sizing and Noise Margin Calculation.
(5) Understand the switching characteristics and interconnect effects of MOS inverters.
(6) Understand the implications of internal and external loading.
(7) Design, implement and simulate: Buffer Chains used to drive big loads.
(8) Understand Combinational MOS logic circuits.
(9) Understand Sequential MOS logic circuits.
(10) Understand Dynamic logic circuits.
(11) Understand the working of ROM and RAM.

(12) Understand limitations of the technology: Short channel effects.
(13) Understand the use of chip I/O circuits.
(14) Understand the design for manufacturability and testability.
(15) Design, implement and simulate: Sequential circuits
(16) Understand the fundamental concepts and technology implications of very short channel devices
(17) Achieve proficiency with aspects of Cadence design suite.

Course Resources

- **Text Book (strongly recommended):**
  Digital Integrated Circuits - A Design Perspective, Second Edition. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Prentice Hall. ISBN 9780130909961.

- **Text Book (optional):**
  CMOS VLSI Design: A Circuits and Systems Perspective, Fourth Edition. Neil Weste, David Harris. ISBN 9780321547743.

- Announcements, course material, tutorials, and other useful links will be posted on Blackboard (http://learn.bu.edu/)

Evaluation

Grading criterion:	Two midterm exams - 15% each, Final Exam – 30%, Project - 20%, Homeworks and Lab Assignments - 20%.
Homework:	Homework assignments are to be submitted before the beginning of the class on the date specified. You can discuss your work in abstract with other students in the class, but you should write-up the solutions on your own.
Exams:	There will be two midterm exams and one final exam.
Project:	Details will be discussed in class and recitation/lab session.

Course Policy

- **Homework**: The homework assignments must be the result of your individual work. You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and write the solutions of homework problems by yourself. Copying the solution and/or answer from another student is considered cheating. Two identical homeworks with same mistakes are considered cheating. **No extensions on homeworks will be provided. Homework received up to 24 hours late will receive maximum 50% credit. Homework received beyond 24 hours late will not be accepted.**

- **Makeup exams**: Makeup exams will be provided if the student takes prior permission from the instructor. Emergencies will be dealt on a case-by-case basis. Note that oversleeping, being not ready, overload due to projects or coursework in other classes **are not valid excuses** for requesting a makeup exam.

- **Exam/Homework grade discussion**: Grade discussion/corrections should be done within one week after the graded exam or homework is distributed. No grade changes will be made after one week, or after the last day of class.

- **I and W grades**: As per University policy.

- **Honor Code**: It is expected that Boston University's Honor Code will be followed in all matters relating to this course. If you are found cheating on homeworks or examinations, you will be brought up on charges before the **Student Academic Conduct Committee** whose punishment may include suspension from the University without the right to transfer credits for courses taken elsewhere.

- Students are responsible for understanding the University's Honor Code policy and must make proper use of citations of sources for writing papers, creating, presenting, and performing their work, taking examinations, and doing research.

- Full text of the honor code policy and fundamental standard: Boston University's Academic Conduct Code

Tentative Schedule for EC571 – Lectures, Recitation/Lab Sessions, Homeworks, Project, and Exams					
Lec #	**Date**	**Topic Description**	**Text Ref**	**Out**	**Due**
1	1/22	Course Introduction	Chapter 1		
2	1/27	CMOS Transistor Theory	Chapter 2, 3		
3	1/29	Non-ideal Transistor Theory, Gates, Pass Transistors	Chapter 3	Hw1	
Lab 1	1/31	Recitation / Lab Session			
4	2/3	Interconnect Parameters and Electrical Wire Models	Chapter 4		
5	2/5	CMOS Inverter Design and Analysis - I	Chapter 5	Hw2	Hw1
Lab 2	2/7	Recitation / Lab Session			
6	2/10	CMOS Inverter Design and Analysis - II	Chapter 5		
7	2/12	Combinational Logic Gates - I	Chapter 6	Hw3	Hw2
Lab 3	2/14	Recitation / Lab Session			
	2/17	No Class: Presidents' Day Holiday			
	2/18	No Class: ISSCC 2025			
	2/19	No Class: ISSCC 2025 (Make up on 4/4)			
Lab 4	2/21	Recitation / Lab Session			
8	2/24	Combinational Logic Gates - II	Chapter 6		
9	2/26	Combinational Logic Gates - III	Chapter 6	Hw4	Hw3
Lab 5	2/28	Recitation / Lab Session: Project Description			
10	3/3	Power and Energy Consumption	Lecture Notes		
11	3/5	**Exam 1**			
	3/10	No Class: Spring Break			
	3/12	No Class: Spring Break			
	3/14	No Recitation / Lab Session: Spring Break			
12	3/17	Sequential Logic Circuits - I	Chapter 7		

13	3/19	Sequential Logic Circuits - II	Chapter 7	Hw5	Hw4
Lab 6	3/21	Recitation / Lab Session			
14	3/24	Sequential Logic Circuits - III	Chapter 7		
15	3/26	Interconnect: Capacitive, Resistive, and Inductive Parasitics	Chapter 9		
Lab 7	3/28	Recitation / Lab Session			
16	3/31	Memory – I	Chapter 12		
17	4/2	Memory – II	Chapter 12	Hw6	Hw5
18	4/4	Make-up Lecture during Lab Section			
19	4/7	**Exam 2**			
20	4/9	Memory – III	Chapter 12		Hw6
Lab 8	4/11	Recitation / Lab Session			
21	4/14	Project Presentations			
22	4/16	Project Presentations			
Lab 9	4/18	Recitation / Lab Session			
	4/21	No Class: Patriots' Day Holiday			
23	4/23	Project Presentations			
Lab 10	4/25	Recitation / Lab Session			
24	4/28	Project Presentations			
25	4/30	Final Exam Review			
	TBD	**Final Exam**			