EC 578  FABRICATION TECHNOLOGY OF INTEGRATED CIRCUITS

Prerequisite: EC 410 or equivalent

Professor: Kleptsyn

Class hours: MW 4:30-6:15

Office hours: W 10:00-12:00

Credits: 4

Maximum number of students 12

Books (recommended):

Also recommended:
Richard C. Jaeger. Introduction to Microelectronic Fabrication. 2002
James D. Plummer, Michael D. Deal, Peter B Griffin. Silicon VLSI Technology. 2000
S.K.Ghandhi. VLSI Fabrication principles 1996.

COURSE CONTENTS

2. Bands, band structure, doping, band gap levels.
4. Silicon processing review (wafer level).
6. Photolithography and masks. Mask design and fabrication.
7. Photoresist processing, BOE etching, photoresist removal.
8. Phase diagrams, solid solubility. Diffusion, Fick’s laws, diffusion from an unlimited and limited sources; interstitial and substitutional diffusion, diffusion coefficient, activation energy. Design of the diffusion process.
9. BJT design and fab. Field effect, MOSFETs. MOSFET design and fabrication steps.
10. Silicon wet etching and reactive ion etching. DRIE.
13. Miscellaneous and auxiliary techniques.
14. Measurement and characterization techniques

In the lab section students will use their theoretical background to process semiconductor devices (wafer level) and acquire the skills needed to do research on solid state devices.
PROJECT

In this course the practical aspects of the fabrication process are the main focus of attention. Basics and theoretical aspects including calculations of the physical processes and parameters will be given and considered accordingly.

The first and the main goal of this course is to guide students through the practical steps of making an integrated circuit of their own design. As a rule, those steps including measurements and inspection will be supposed to perform manually for more profound understanding of the physical and chemical processes.

The project consists of three main portions:

1. Design. Students will have to design a circuit (e.g. amplifier), transistors, masks and technological process of the fabrication on the wafer level.
2. Processing. Students will perform all necessary technological steps starting with plain wafer; the wafer containing a few hundred patterned chips should be presented at the end of the course.
3. Inspections and tests will have to be done after each technological step/operation. Final wafer inspection may include measurements and characterization.

Grading: Homework 20%, Labwork (project) 40%, Final exam 40%.

Academic Misconduct
BU takes academic integrity very seriously. Academic misconduct is conduct by which a student misrepresents his or her academic accomplishments, or impedes other students’ opportunities of being judged fairly for their academic work. Knowingly allowing others to represent your work as their own is as serious an offense as submitting another’s work as your own. More information on BU’s Academic Conduct Code, with examples, may be found at http://www.bu.edu/academics/policies/academic-conduct-code.

Collaboration Policy
In this class you may use any textbooks or web sources when completing your homework, and collaborators from class, subject to the following strictly enforced conditions:
You must clearly acknowledge all your sources (including your collaborators) on the top of your homework.
You must write all answers in your own words.
You must be able to fully explain your answers upon demand (and I will demand it!).
Obviously, you may not collaborate with anyone on exams.
Failure to meet any of the above conditions could constitute plagiarism and will be considered cheating in this class. If you are not sure whether something is permitted by the course policy, ASK ME! (it’s much more awkward to explain your actions after the fact to the college disciplinary committee).