EC571/Digital VLSI Circuit Design
Fall 2023
Lecture: Mon-Wed 12:20 pm – 2:05 pm in CDS 262
Recitation/Lab: Friday 12:20 pm – 2:05 pm in PHO 305
Number of credits: 4, Prerequisites: EC 311, EK307, EC 410 (optional)

Course Objective
The objective of this course is to learn how to design digital CMOS circuits and digital VLSI systems for given area, power, performance, and reliability specifications.

Staff Information
Instructor:
Ajay Joshi
Email: joshi@bu.edu (Make sure you include EC571 in the subject line).
Office Hours: Friday 10 am to 11 am in PHO 334.

Graduate Teaching Fellow
Dingning Li
Email: dingning@bu.edu (Make sure you include EC571 in the subject line).
Office Hours: Tuesday 6:30 pm to 7:30 pm in PHO 305.

Grader/Lab Assistant:
David Liu
Email: liudavid@bu.edu (Make sure you include EC571 in the subject line).

Textbooks and Class Material
4. Announcements, course material, and other useful links will be posted on Blackboard (http://learn.bu.edu).
5. Piazza should be used for posting questions: (http://www.piazza.edu).
6. Gradescope will be used for submitting and grading homework (http://www.gradescope.edu).

Course Goals
To provide students with:
1. Extensive training in the design of CMOS integrated circuits that perform an arbitrary digital function and meet an arbitrary performance specification.
2. Hands-on experience to become proficient with VLSI CAD tools.
3. Understanding of how to keep pace with the field as it crosses into “new territory” over the next few years.
**Course Outcomes**

As an outcome of completing this course, students should be able to:

1. Understand the MOSFET basics and their fabrication and the layout design rules.
2. Understand the operation of the MOS transistor.
3. Understand the static characteristics of MOS inverters.
5. Understand the switching characteristics and interconnect effects of MOS inverters.
6. Understand the implications of internal and external loading.
7. Design, implement, and test: Buffer Chains used to drive big loads.
8. Understand Combinational MOS logic circuits.
9. Understand Sequential MOS logic circuits.
10. Understand Dynamic logic circuits.
11. Understand the working of ROM and RAM.
12. Understand limitations of the technology: Short channel effects.
13. Understand the use of chip I/O circuits.
14. Understand the design for manufacturability and testability.
15. Design, implement and test: Sequential circuits
16. Understand the fundamental concepts and technology implications of very short channel devices
17. Achieve proficiency with aspects of the Cadence tool suite.

**Evaluation**

**Grading**

Three mid-term exams: 60% total (20% each), Homeworks: 24% total (3% per Homework), Project: 16%.

**Exams**

The mid-term exams will be during class time.

**Project**

We will do a group project at the end of the semester. Each group will consist of 3 students. Details of the project will be provided at a later date.

**Homeworks**

Homework assignments will consist of a pencil-paper component and/or a lab component. Homeworks are to be submitted before the beginning of the class on the date specified. You can discuss your work in abstract with other students in the class, but you should write up the solutions on your own.
**Course Policies**

**Pencil-Paper Component of the Homework:**
The pencil-paper component of the homework assignments must be the result of your individual work. You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and write the solutions to homework problems by yourself. Copying the solution and/or answer from another student is considered cheating. Two identical homeworks with the same mistakes are considered cheating. No extensions on homeworks will be provided.

**Lab Component of the Homework:**
The lab component of the homework assignments must be the result of your work. You can discuss your approach for completing the lab component with others, but not the detailed solution. Note that all lab components are to be submitted via Git Hub. We will compare each lab submission with other lab submissions. If we come across two solutions that are identical or closely match each other, then that will be considered cheating. No extensions on labs will be provided.

**Makeup exams:**
Makeup exams will be provided if the student takes prior permission from the instructor. Emergencies will be dealt with on a case-by-case basis. Note that oversleeping, being not ready, overloaded due to projects or coursework in other classes are not valid excuses for requesting a makeup exam.

**Exam/Home Grade discussion:**
Grade discussion/corrections should be done within one week after the graded exam or homework is distributed. No grade changes will be made after one week, or after the last day of class.

**I and W grades:**
As per University policy.

**Academic Integrity and Honor Code:**
- Your submission of the homework assignments must be the result of your individual work. You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and write the solutions by yourself. Copying the solution and/or answer from another student or source is considered cheating.
- Clearly reference any sources you used in your work: books, the Internet, and your collaborators!
- Boston University’s academic code of conduct will be strictly applied.
- Boston University’s computing ethics will be strictly applied.
# Course Schedule (subject to change)

<table>
<thead>
<tr>
<th>Lecture Number</th>
<th>Date</th>
<th>Lecture Topic</th>
<th>Text Reference (Rabaey et al.)</th>
<th>Homework Due</th>
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<tbody>
<tr>
<td>1</td>
<td>Sep 6</td>
<td>Introduction, MOS Manufacturing, Design rules</td>
<td>Chapter 1, 2</td>
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<td>2</td>
<td>Sep 11</td>
<td>CMOS Inverter Design and Analysis - I</td>
<td>Chapter 5</td>
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<td>Sep 13</td>
<td>CMOS Inverter Design and Analysis - II</td>
<td>Chapter 5</td>
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<td>Sep 18</td>
<td>Transistor Modeling - I</td>
<td>Chapter 3</td>
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<td>Transistor Modeling - II</td>
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<td>Wire Modeling</td>
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<td>7</td>
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<td>Memory - I</td>
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