BOSTON UNIVERSITY

EC551 - Advanced Digital Design with Verilog and FPGAs
Fall 2022

Class: Tuesday and Thursday, 1:30pm – 3:15pm in MCS B37
Lab: Section N/A, Monday 4-6pm, Wednesday 2-4pm, and Friday 4-6pm in PHO 115
Number of credits: 4, Prerequisites: EC311, EC413

Course Objectives

Content includes the use of a hardware description language (HDL; in particular Verilog) for the specification, synthesis, simulation, and exploration of principles of register transfer level (RTL) designs. Programmable logic, such as field programmable gate array (FPGA) devices, has become a major component of digital design. In this class the students learn how to write HDL models that can be automatically synthesized into integrated circuits using FPGAs. Laboratory and homework exercises include writing HDL models of combinational and sequential circuits, synthesizing models, performing simulation, writing testbench modules, and synthesizing designs to an FPGA by using automatic place and route EDA tools.

The course material is broken down in to four areas: Electronic Design Automation (EDA), Verilog, Reconfigurable Computing (RC), and the course Project. The topics are scheduled and organized so that these topics are woven together in lecture to provide breadth and depth in select areas. Homework (HW) and Lab exercises are created to reinforce lecture material and provide the required knowledge for the larger course project. At the conclusion of the course, the students should understand a digital EDA design flow and how to program reconfigurable computing hardware using this flow.

The course project plays a major role in the course. Students are expected to create a fully demonstrable digital system on an FPGA. This project is done in groups of 4-5 students and should represent 15 hours of work (or more) per student per week.

Staff Information

Instructor
Name: **Prof. Douglas Densmore**
Office: **CILSE 403**
Office phone number: 617-358-6238
E-mail address: dougd@bu.edu (**Best way to contact me - Include EC551 in the subject line**)
Office Hours: CILSE 403, Tuesdays 4pm-5pm, Thursdays 4pm-5pm or by appointment
Zoom Link: https://bostonu.zoom.us/j/4602829913

Lab Assistant
Name: Guowei Yang
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Office Hours: 4pm - 6pm Wednesdays in PHO 340 or by appointment
Grader
Abinaya Senthil
Email Address: abisen98@bu.edu (**Include EC551 in the subject line**)

Course Resources

Required Textbooks

1. Author: M.D. Ciletti
   Title: Advanced Digital Design with the Verilog HDL (2nd Edition)
   ISBN: 0136019285

Optional Textbooks

1. Author: David R. Smith, Paul Franzon
   Title: Verilog Styles for Synthesis of Digital Systems
   ISBN: 0201618605

2. Author: Samir Palnitkar
   Title: Verilog HDL
   ISBN: 0132599708

Announcements, course material and other useful links

Will be posted on Blackboard Learn (http://learn.bu.edu)

- EC551/Fall 2022

We will also use Piazza as a forum for questions on HW, labs and the class project

Goals

To provide students with:

- An experience of how to write HDL models that can be automatically synthesized into integrated circuits using programmable hardware such as FPGAs.
- An understanding of how to take a electronic design from concept to register transfer level (RTL) verification and synthesis to final programmable device implementation.
- An experience in writing HDL models of combinational and sequential circuits, synthesizing models, performing simulation, writing test modules, and fitting designs within resource, power, and timing constraints of an FPGA by using automatic place and route CAD software.

Course Outcomes

As an outcome of completing this course, students should be able to:

- Understand advanced topics in digital logic design
- Understand proven design methodologies based on standard EDA tools
- Understand the differences and similarities in hardware and software design
- Understand modern specification methods (HDL)
- Design combinational devices with a full set of EDAtools (skills)
- Understand modeling and verification with hardware description languages
- Understand synthesis with HDLs
- Understand programmable logic devices and FPGAs
- Design state machines, datapath controllers, and assorted CPUs with a full set of EDA tools
- Understand timing analysis
- Understand fault simulation and testing

Evaluation
Grading

Midterm - 10%
Final Exam - 10%
Final Project - 40%
Labs (3) - 30%; (10%, 10%, 10%)
Five Homework Assignments - 10% (2% each)

Class participation will help your grade if you are on the border of a grade (e.g. B+ to A-). Class participation includes but is not limited to answering questions in class, attending offices hours, helping others when appropriate in the lab, and serving in a leadership role in your project group.

Homework

Homework assignments will be posted on the Blackboard website **two or more weeks ahead of their due dates**. Homework is to be submitted outside of CILSE 403 or in class **before** the beginning of the lecture **(1:30 sharp)** on the date specified. You can discuss your work **in the abstract** with other students in the class, but you **must** write-up the solutions on your own.

Labs

Lab descriptions will be posted on the Blackboard website **two or more weeks ahead of their due dates**. Lab assignments are done in groups of **two students**. **Labs are due via email at 11:59pm on the due date.** You may remain in the same group for the whole semester or change groups with each lab. This is up to you. **Any partner conflicts should be reported EARLY to Prof. Densmore.**

Exams

There will be one midterm exam and a final exam. **The midterm will be 1:30-3:15pm in class. If you are unable to attend this date, you must provide 1 week advance notice along with appropriate documentation.** The final exam will be **?? from ??pm in ??**. Make up exams will only be given under extreme circumstances.

Project

Projects will be done in groups of four students (three and five person groups will be allowed in extreme circumstances). **The project will represent a SIGNIFICANT amount of work and will culminate in a demonstrable digital system running on an FPGA.** There will be three project presentations and one demo session. The first two will be 10 minute, in class updates. **Final project presentations will be during the last weeks classes and all team members must be present (see schedule).** Project presentations will be done in front of all students and should be treated as a professional presentation. More information regarding the projects will be provided during the semester. The project demo is the last day of class. Arrangement for the schedule and process of project demos will be made available later in the semester.

Previous project videos can be found at:
https://www.youtube.com/channel/UCPYhfQlY30fTfEg7LpRPQtw

Course Policy

- Homework/Lab: The homework assignments must be the result of your individual work (HW) or you and your partner (labs).

- You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and to write the solutions of HW/Lab problems by yourself/group. Copying the solution and/or answer from another student is considered cheating. Two identical HWs/Labs with same mistakes are considered cheating. **No extensions on homeworks or labs will be provided. If you will be absent on a day they are due you should make arrangement in advance with Prof. Densmore.**

- Makeup exams: Makeup exams will be provided if the student receives **prior permission** from the instructor. Emergencies will be dealt on a case-by-case basis. Note that oversleeping, being not ready, or overload due to projects or coursework in other classes are **not** valid excuses for requesting a makeup exam.

- Exam/Home/Lab Grade discussion: Grade discussion/corrections should be done within one week after the graded exam of homework is distributed. **No grade changes will be made after one week, or after the last day of class.**

- I and W grades: As per University policy.

- Honor Code: If you are found cheating on HWs, labs, or examinations, you will be brought up on charges before the Student Academic Conduct Committee whose punishment may include suspension from the University without the right to transfer credits for courses taken elsewhere.

Schedule for EC551 Fall 2022 - Lectures, Homework, Labs and Exams					
Lecture #	**Date**	**Topic Description**	**Labs Out/Due**	**Hw Out**	**Hw Due**
1	9/6 (T)	Course Introduction			
2	9/8 (Th)	**EDA** - Review of combinational logic		THQ1&2	
3	9/13 (T)	**EDA** - Review of sequential logic			
4	9/15 (Th)	**EDA** – Quiz review and grading			THQ1&2
5	9/20 (T)	**Verilog** - Structural Verilog and Hierarchy	Prelab	HW1	
6	9/22(Th)	**Verilog** - Simulation and Test			
7	9/27 (T)	**RC** – FPGAs + Paper 1 Out			
8	9/29 (Th)	**Verilog** - Behavioral Verilog	Lab1/Prelab (Fri)		
9	10/4 (T)	**Project** - Plan and Goals Presentations		HW2	
10	10/6 (Th)	**RC** - Paper Review 1 + Paper 2 Out			HW1
11	**10/13 (Th)**	**EDA** - Synthesis - Scheduling/Control			
12	10/18 (T)	**Midterm (in class)**		HW3	
13	10/20 (Th)	**EDA** - Synthesis – ASMs	Lab2/Lab1 (Fri)		HW2
14	10/25 (T)	**EDA** - Synthesis - Multi-Level Logic			
15	10/27 (Th)	**RC** - Paper Review 2 + Paper 3 Out			
16	11/1 (T)	**EDA** – Tool Review + Demo		HW4	
17	11/3 (Th)	**Project** - Review and Update Presentations	Lab3/Lab2 (Fri)		HW3
18	11/8 (T)	**EDA** - Static Timing Analysis			
19	11/10 (Th)	**Verilog** - IP Cores and Microarchitecture			
20	11/15 (T)	**RC** - Paper Review 3 + Paper 4 Out		HW5	
21	11/17 (Th)	**EDA** - Retiming	Lab3 (Fri)		HW4
22	11/22 (T)	**EDA** - Design for Test/ Testing			
		Thanksgiving Break			
23	11/29 (T)	**EDA** – Physical Design			
24	12/1 (Th)	**RC** - Paper Review 4			
25	12/6 (T)	**Project** - Final Presentations 1	Project Group1		
26	12/8 (Th)	**Project** - Final Presentations 2	Project Group2		HW5
27	**?? (??)**	**Final Exam – ??pm in ??**			