BOSTON UNIVERSITY
COLLEGE OF ENGINEERING

Department of Electrical and Computer Engineering

EC410 – Introduction to Electronics
Fall Semester 2021

Section	A1	Dis.	Lab
Instructor	Prof. M.C. Lee mclee@bu.edu	GTA: Ashley Antony Gomez ashleyag@bu.edu	GTA/UTAs
Time	M/W 2:30-4:15 PM	B1 TR 8-8:45 AM WED 205	C1 F 8:00-9:45 AM
Classroom	EPC 204	B2 W 4:40-5:30 PM PSY B50	C2 TR 1:30-3:15 PM
Office Hours	TBA (via zoom)	B3 W 12:20-1:10 PM WED 210	C3 F 12:20-2:05 PM
Office Loc	PHO 418	B4 TR 6:30-7:20 PM KCB 201	C4 Tue 6:30-8:15 PM

Course Description:
Discussion of 2-terminal and 3-terminal non-linear and active devices; power supply circuits; simple linear amplifier circuits including biasing, incremental analysis, large-signal analysis, and frequency response; introduction to digital circuits. (4 credits)

Prerequisite: ENG EK307

Text: M. Horenstein, *Microelectronic Circuits and Devices*, 2nd edition, Prentice-Hall, 1996
Lab Manuel: See https://sites.bu.edu/engcourses/ec410/

References:
1. Jaeger and Blalock, *Microelectronic Circuit Design*, McGraw-Hill, 2003
2. Attia, *PSPICE and MATLAB for Electronics*, CRC Press, 2002

Course Content:
EC410 includes a coordinated set of lectures, labs, homework, and exams to provide students with an introduction to electronics and circuit design. Lab sessions meet weekly in PHO105 where students will perform a variety of introductory circuit experiments using components and a breadboard (previously purchased in kit form for EK307). Each lab session will be conducted by GTA/UTA assigned to the course. Students will also be assigned weekly discussion times with a GTA to discuss the course material and ask questions on the homework. The course will contain two mid-terms and a final exam.

Grading:	Mid-term Exam I	20%
	Mid-term Exam II	20%
	Labs	15%
	Homework	15%
	Final Exam	30%

Schedule of Lectures and Exams:

Dates	***Topic Description***	***Text Material***
9/8	Course intro, linear ckts review, KVL, KCL, superposition	1.1 – 1.5
9/13	Thevenin Eq ckts, current & voltage divider, RC/RL ckts,	1.6 - 1.9
9/15	Transformers, Op-Amps ckts., Phasors/AC steady-state	notes
9/20	Non-linear ckts, graphical method, PN junction diode	3.1 – 3.3.2
9/22	PN diode circuits; Zener, tunnel, varactor, & Schottky diodes	3.3.3 – 3.3.9
9/27	Graphical methods, iterative solution, piece-wise linear modeling	3.4 - 3.6
9/29	Diode circuits: clipping, limiting	4.1 – 4.2
10/4	Rectifier circuits: half-wave rectifier, bridge rectifier	4.3 – 4.4.2
10/6	Power supply circuits, voltage regulator, detector circuit	4.4.3 – 4.4.5
10/12	Precision rectifiers, FET Devices, load line, NMOS depletion mode	4.5, 5.1 – 5.2.3
10/13	Body effect, transconductance, PMOS	5.2.4, 5.2.5, 5.2.7, 5.2.8
10/15	**Mid-Term Exam I**, **Friday, 6-8 PM**	
10/18	Bipolar junction transistors	5.3
10/20	Drain and collector resistance, Early Voltage	5.4
10/25	Photonic devices, temperature dependence, power limitations	5.5 – 5.7
10/26	Transistor Circuits - inverters (common emitter, common source)	6.1
10/27	Transistor Circuits – voltage follower (emitter flwr, source flwr)	6.2
11/1	Transistor Circuits – current follower (gnd'ed base, gnd'ed gate)	6.3
11/3	Basic analog amplifier circuits: voltage gain, power gain	7.1 – 7.2
11/8	Biasing MOSFET amplifiers, BJT small-signal models	7.3
11/10	BJT and MOSFET small-signal models, Review	7.4
11/15	Two-port representation, Frequency response, circuit capacitance	7.5, 9.1
11/17	Sinusoidal steady-state response, Bode plot, Review	9.2
11/19	**Mid-Term Exam II, Friday, 6-8 PM**	
11/22	Capacitors affecting high/low freq response, dominant pole	9.3.1 – 9.3.2
11/29	Transverse capacitance, Miller's Theorem	9.3.3 – 9.3.4
12/1	High freq poles with feedback, Freq response with bypass capacitor	9.3.5 – 9.3.6
12/6	Digital circuits: logic levels, noise margin, delay,	6.4, 14.1
12/8	CMOS, NMOS; review of the final exam	14.2 – 14.3
TBA	**Final Exam**	

	Lab Schedule
9/6	No Lab
9/13	Intro to Equipment, Pspice (http://sites.bu.edu/engcourses/ec410/)
9/20	Diode V-I Characteristics
9/27	Diode Circuits
10/4	Power Supplies

10/11	No Lab
10/18	I-V Characteristic of MOSFET
10/25	I-V Characteristic of BJT
11/1	MOSFET Amplifier (see Analog Amplifier Design)
11/8	BJT Amplifier (see Analog Amplifier Design)
11/15	Transistor Curve Tracer
11/22	No Lab
11/29	MOSFET Differential Amplifier
12/6	Make Up Sessions

Rules for the SC410 Laboratory:
A bound 8½ x 11 lab notebook should be used to record all relevant data in it. Do not use loose-leaf data sheets in the lab. Each lab will need to be signed off by a EC410 GTA.

Course Policies:

1. Lectures – Attendance in class is considered essential and required.
2. Exams – Absence from an exam can be excused only for reasons of illness, or unavoidable travel. In each case, permission of the instructor in advance is required, as well as a written authorization by a physician (in the case of illness) or other appropriate authorized signature.
3. Homework – Late homework will not be accepted.
4. Labs – Late lab reports will not be accepted.