EC311/Introduction to Logic Design
Fall 2021

Class: Mon and Wed 12:20 pm to 2:05 pm in PHO 203
Labs: Mon 10:10 am to 11:55 am, Wed 4:30 pm to 6:15 pm,
Thu 3:30 pm to 5:15 pm, and Fri 12:20 pm to 2:05 pm.

Course Objective

The class covers the theory and practice of digital hardware design. Students will learn to formulate real world tasks using Boolean algebra and FSM theory, and to apply manual and computer-aided techniques to solve the problems. In addition, they will also learn fundamental logic design and verification skills using Verilog HDL and FPGAs.

Staff Information

Instructor:
Ajay Joshi
Email: joshi@bu.edu (Include EC311 in the subject line).
Office Hours: 5:30 pm ET to 6:30 pm ET on Tuesday via Zoom or by appointment.

GTFs:
Cansu Demirkiran
Email: cansu@bu.edu (Include EC311 in the subject line).
Office Hours: Wednesday 7:00 pm ET to 8:00 pm ET and Friday 3 pm ET to 4 pm ET or by appointment in PHO 115.

UTFs
Abin Binoy George (abg309@bu.edu)
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Textbooks and Class Material

Digital Design, Sixth Edition, Mano and Ciletti, Pearson (5th edition is also acceptable).
Starter's Guide to Verilog 2001, Ciletti. Pearson.

Assignments, announcements, course material, updated schedule, and other useful links will be posted on Blackboard (http://learn.bu.edu) and/or Piazza (https://piazza.com/). Please use Piazza for asking questions.

Course Goals

To provide students with:

- An experience with digital logic implementation.
- An understanding of the CAD tools used for logic design.
- An understanding of sound logic design methodologies.

Course Outcomes
As an outcome of completing this course, students should be able to:

- Understand the applications of logic design
- Understand abstraction and hierarchy in digital design
- Understand what components are available for logic design
- Understand the use of Boolean algebra in logic analysis and design
- Understand logic minimization criteria and methods for use in design
- Understand the concept of state in digital systems
- Design combinational digital logic systems given specifications
- Design sequential digital logic systems (finite state machines) given specifications
- Implement logic designs in hardware and with CAD tools
- Discover component availability and data using the Internet or other resources

Evaluation
Grading
Two in-class exams: 15% each, One final exam: 25%, Project: 14%, Labs: 15%, Homework: 16%.

Exams
The first two exams will be during class time. The third exam will take place during the scheduled final exam timeslot.

Project
We will do a group project at the end of the semester. Each group will consist for 4-5 students. Details of the project will be provided at a later date.

Labs
Lab assignments will be posted on the Blackboard website. Grades will be assigned to completed labs. Students are expected to attend their scheduled lab section every week.

Homeworks
Homework assignments will be posted on the Blackboard website. Homeworks are to be submitted before the specified deadline. No credit will be given for late homework

Course Policies
Exam/Homework/Lab Grade discussion:
Grade discussion/corrections should be done within one week after the graded exam or homework is distributed. No grade changes will be made after one week.

Collaboration Policy:
In this class you may use any textbooks or web sources when completing your homework, and/or one human collaborator (from class) per homework, subject to the following strictly enforced conditions:

- You must clearly acknowledge all your sources (including your collaborators) on the top of your homework.

- You must write all answers in your own words.
- You must be able to fully explain your answers upon demand (and I will demand it!).
- You may not use any human resource outside of class (including web-based help services, outside tutors, etc.) in doing your homeworks or project. Obviously, you may not collaborate with anyone on exams.

Failure to meet any of the above conditions could constitute plagiarism and will be considered cheating in this class. If you are not sure whether something is permitted by the course policy, ASK ME! (it's much more awkward to explain your actions after the fact to the college disciplinary committee).

Academic integrity:

- Boston University's academic code of conduct will be strictly applied.
- Boston University's computing ethics will be strictly applied.

Course Schedule

Lecture Number	Date	Lecture Topic	Reading Chapters (Mano)	Homework Due	Lab Out
1	Sep 8	Introduction	1.1-1.6		
2	Sep 13	Numbers, binary arithmetic, gates	1.6-1.9		Pre-Lab A
3	Sep 15	Boolean algebra, canonical forms	2.1-2.8		
4	Sep 20	K-Maps, logic minimization	3.1-3.5	Hw 1	Pre-Lab B
5	Sep 22	Gate implementation	3.6-3.8		
6	Sep 27	Verilog	3.9	Hw 2	Lab 1
7	Sep 29	Combinational logic	4.1-4.5		
8	Oct 4	Adders, multipliers, comparators	4.5-4.8	Hw 3	
9	Oct 6	Decoder, encoders	4.9-4.10		
10	Oct 12	Encoders, MUXes	4.10-4.11	Hw 4	
11	Oct 13	MUXes, tri-state	4.10-4.12		
12	Oct 18	**Exam 1**			
13	Oct 20	Synchronous sequential logic: latches and FFs	5.1-5.4		Lab 2
14	Oct 25	State machines	5.5-5.7		
15	Oct 27	State assignment, synthesis	5.7-5.8		
16	Nov 1	State assignment, synthesis	5.7-5.8	Hw 5	

Lecture Number	Date	Lecture Topic	Reading Chapters (Mano)	Homework Due	Lab Out
17	Nov 3	Registers	6.1-6.3		
18	Nov 8	Counters	6.4-6.6	Hw 6	
19	Nov 10	Memory	7.1-7.2		
20	Nov 15	Error codes	7.3-7.4	Hw 7	
21	Nov 17	ROM, PLD, PLA, PAL	7.5-7.8		
22	Nov 22	**Exam 2**			
23	Nov 29	Pipelining			
24	Dec 1	Processor basics		Hw 8	
25	Dec 6	Project presentations			
26	Dec 8	Project presentations			
	TBD	**Final Exam**			