Fifth Annual Boston Area Architecture Workshop

Advance Program

Friday, January 26, 2007
Boston University
Photonics Center Building, 9th Floor
8 Saint Mary's Street, Boston, MA

9:00am - 9:25am Continental Breakfast

9:25am - 9:30am Welcome by Dean Kenneth Lutchen, BU Engineering College

9:30am - 10:10am Session 1, Invited Talk
Exploring the Cell with HPEC Challenge Benchmarks
Jeremy Kepner, MIT Lincoln Laboratory

10:10am - 11:10am Session 2, Parallel Architecture
Chair: David Kaeli, Northeastern University
The Scale Vector-Thread Processor
Ronny Krashinsky, Christopher Batten, Krste Asanovic, MIT

Investigating Energy/Performance Tradeoffs using Transactional Memory in a MPSoC Environment
Cesare Ferri, Brown University; Tali Moreshet, Swarthmore College; R. Iris Bahar, Brown University; Luca Benini, University of Bologna; Maurice Herlihy, Brown University

Pipelining the Connex Array
Dominique Thiebault, Smith College; Mihaela Malita, St. Anselm College

11:10am - 11:40am Poster Session, Coffee Break

An Asynchronous NoC Router Architecture Supporting Quality-of-Service
Youngbok Kim, Yong-Bin Kim, Northeastern University

Cache Hierarchy for 100 On-Chip Cores
Mohamed Zahran, City University of New York

Stream Programming on the Blackfin Architecture
Michael G. Benjamin, David Kaeli, Northeastern University

A Case for Active Storage Networks in High Performance Computing
John Chandy, University of Connecticut
Modeling and Evaluation of Multi-Bank SRAM Design for Leakage Power Reduction
Byunghyun Jang, Yong-Bin Kim, Northeastern University

Custom Register Binding in Application-Specific Instruction Set Processors to Eliminate Register Spills
Hai D. Lin, Yunsi Fei, University of Connecticut

Characterizing the Relationship Between Sparse Matrix Preconditioners and the Storage Hierarchy
Diego Rivera, David Kaeli, Northeastern University; Misha Kilmer, Tufts University

Case Study: Soft Error Rate Analysis in Storage Systems
Brian Mullins, Hossein Asadi, Mehdi Tahoori, David Kaeli, Northeastern University; Kevin Granlund, Rudy Bauer, Scott Romano, EMC

NASICs with Nanoscale Built-In Error-Correction
Teng Wang, Michael Leutenberg, Pritish Narayana, Csaba Andras Moritz, University of Massachusetts

11:40am - 1:00pm Session 3, Design and Technology
Chair: R. Iris Baha, Brown University

Communications for Multicore Processors
James Psota, Jonathan Eastep, Jason Miller, Theodoros Konstantakopoulos, Michael Watts, Mark Beals, Jurgen Michel, Kim Kimerling, Anant Agarwal, MIT

Designing Memory Subsystems Resilient to Process Variations
Mahmoud Bennaser, Csaba Andras Moritz, University of Massachusetts, Amherst

Soft-Redundancy Allocated Cache Microarchitecture
Shuo Wang, Lei Wang, University of Connecticut

VLIW with Variable Partitioning and Threading: A Multithreaded Architecture
Tom VanCourt, Altera

1:00pm - 2:00pm Lunch

2:00pm - 2:40pm Session 4, Invited Talk
Power/Performance Tradeoffs in Microprocessor Design
Dan Leibholz, AMD

2:40pm - 3:40pm Session 5, Architecture
Chair: Yunsi Fei, University of Connecticut

Continuous Data Protection in iSCSI Storage
Qing Yang, Weijun Xiao, Jin Ren, University of Rhode Island
Performance Characterization of SPEC CPU2006 Integer Benchmarks on the x86-64 Architecture
Dong Ye, David Kaeli, Northeastern University

Predicting When a Branch Predictor Will Fail
Resit Sendag, University of Rhode Island;
Peng-fei Chuang, University of Minnesota;
Joshua J. Yi, Freescale Corporation

3:40pm - 4:10pm Poster Session, Coffee/Snack Break
4:10pm - 5:50pm Session 6, Automation and Analysis
Chair: Gus Uht, University of Rhode Island

Statistical Inference for Efficient Microarchitectural Analysis
Benjamin C. Lee, David M. Brooks, Harvard University

Embedding Program Code Integrity Monitoring in Application Specific Instruction Set Processors
Yunsí Fei, Z. Jerry Shi, University of Connecticut

HAsim: Implementing a Partitioned Simulator on an FPGA
Michael Pellauer, MIT; Joel Emer, Intel

Instruction-Level Energy Estimation
Seth Molloy, David Kaeli, Northeastern University

A New Approach to Constructing Portable Instruction-Set Simulators
Wei Qin, Boston University; Joseph D'Errico, Cavium Networks;
Xinping Zhu, Northeastern University

5:50pm - 5:55pm Final Remarks