**ABSTRACT (No. 47)**

This research proposes a novel, low-cost method to reconfigure the on-chip interconnects at runtime to maximize performance and energy efficiency of manycore systems running parallel workloads. We analyze various commonly used cache hierarchies and network topologies. We propose a reconfiguration policy that predicts the energy-delay product (EDP) for the currently running application at various channel widths and chooses the best fitting width to minimize EDP. The experimental results show that our policy reduces EDP by 39.3% and 49.3% for private L2 cache and 65.5% and 23.9% for distributed L2 cache on average in systems with bus and crossbar topologies, respectively, in comparison to statically setting the channel width.

**MOTIVATION**

Manycore Systems
- Have dozens of cores on a single die
- Demand energy efficiency
- Go through significant workload variations during system lifetime

**TARGET SYSTEM AND CONFIGURATIONS**

**Target System**
- 64-core Processor
- 22 nm process with die area of 400 mm²
- 1 GHz core frequency and 0.9 V supply voltage
- Private and distributed L2 cache architectures

**Architectural Configuration**

**PERFORMANCE AND POWER SIMULATION**

**Processor Performance**
- Performance metric: Application IPC
  \[ \text{IPC}_{\text{app}} = \frac{\text{Committed\_Instructions\_out}}{\text{Max\_cas}\_\text{cycle} \times \text{Number\_of\_Cycles\_out}} \]
  - Simulator: M5 full-system simulator [3] with the Alpha ISA, DEC Tsunami system to boot Linux 2.6.
  - Benchmarks: parallel applications from the PARSEC benchmark suite [4] and NAS Parallel Benchmarks (NPB) suite [5].

**Processor Power**
- L2 cache power: CACTI 5.3 [6]
- Core power: McPAT 0.7 [7], utilizing M5 performance results to estimate the run-time dynamic and leakage power.
- Power scaling: McPAT outputs are calibrated to match the published power of Intel 48-core processor:
  \[ P_{\text{L2 dram}} = P_{\text{L2 dram}}^{\text{CACTI 5.3}} \times \left( \frac{V_{\text{core}}}{2.0} \right)^2 \phi \]
- Network Performance and Power
  - 75 mm energy-optimized pipelined channels, 30 pipeline stages
  - 0.6 W to 2.0 W bus power; 25.2 W to 26.6 W crossbar power

**RECONFIGURATION POLICY**

Flowchart of the Run-time Reconfiguration Policy

1. Start application with the initial configuration
2. Collect statistics after each interval (e.g., 10 million cycles)
3. Estimate IPC and predict EDP for all configurations
4. Does the current configuration have the lowest EDP prediction?
   - No
     - Is the program finished?
       - Yes
         - End of the simulation: refine the regression model if necessary
       - No
         - Collect statistics after each interval
         - Does the current configuration have the lowest EDP prediction?
           - Yes
             - Reconfigure with the most suitable interconnect channel-width
           - No
             - Collect statistics after each interval
             - Does the current configuration have the lowest EDP prediction?
               - Yes
                 - Reconfigure with the most suitable interconnect channel-width
               - No
                 - Collect statistics after each interval

**EXPERIMENTAL RESULTS**

**Energy savings for bus topology**
- EDP savings: 20.6% on average (reconfiguration choice)
- EDP reduction for bus topology with private L2 cache architecture

**Energy savings for crossbar topology**
- EDP savings: 39.3% on average (reconfiguration choice)
- EDP reduction for crossbar topology with distributed L2 cache architecture

**REFERENCES**

For more information, please refer to: