PACT: A SPICE-Based Parallel Compact Thermal Simulator for Fast Analysis

Mohammadamin Hajikhodaverdian*, Zihao Yuan*, Sherief Reda†, Ayse K. Coskun*
*Electrical and Computer Engineering, Boston University, USA †School of Engineering, Brown University
{aminhaji, yuan1z, acoskun}@bu.edu, sherief_reda@brown.edu

***Abstract*—Thermal analysis is crucial for designing computing systems alongside their cooling mechanisms. However, existing tools face challenges in addressing large-scale problems and long simulation times. PACT is a SPICE-based parallel thermal simulator capable of fast and accurate simulations from standard-cell to architecture levels. PACT leverages multicore processing and various solvers and can be easily extended to model a variety of cooling and integration technologies. Compared to state-of-the-art tools like COMSOL and HotSpot, PACT offers significant speedups while maintaining accuracy.**

***Index Terms*—Compact thermal models (CTMs), SPICE, standard-cell level thermal simulation, thermal simulation.**

I. Introduction

Chip temperature is a crucial parameter to consider when designing high-performance, reliable, and cost-efficient integrated circuits. High temperatures degrade chip performance and increase sub-threshold leakage power, making thermal simulation an essential part of the chip design process. Existing commercial simulators that rely on finite-element method (FEM)-based multiphysics (e.g., COMSOL and ANSYS) are computationally extensive and require large memories and, therefore, have limited use in circuit or architecture-level design and optimization. Compact thermal modeling (CTM) methods [1] emerged to provide faster yet sufficiently accurate thermal simulation. CTM is based on the duality between thermal and electric properties, where a lumped RC circuit representing the chip's thermal components can be expressed as differential equations and solved.

A challenge with current CTMs is that existing thermal simulators only perform thermal simulation at the architecture level and are not compatible or easy to integrate with the standard-cell level. Also, they cannot efficiently tackle complex designs (e.g., multilayered chips such as large 2.5D chips or monolithic 3D).

PACT [2] is a SPICE-based parallel compact thermal simulator that is fast and accurate in thermal analysis. Unlike existing thermal simulators, PACT supports parallel computing, providing fast and accurate standard-cell level to architecture level simulation, regardless of the problem size. Owing to its modular design, PACT can be easily extended to support various emerging integration and cooling technologies.

PACT has been shown to provide similar accuracy to HotSpot, while providing up to 186× speedup in evaluating transient thermal simulations. In this paper, we highlight key features in the design of PACT, show example case studies, and discuss its latest features.

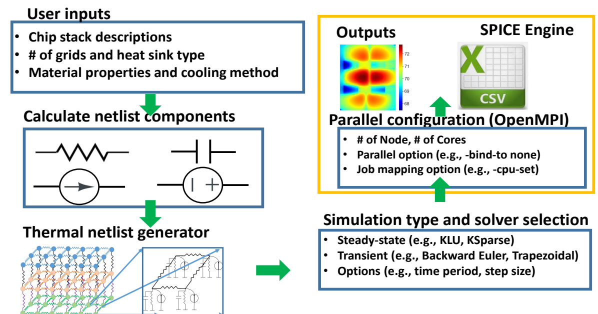

Fig. 1. PACT high-level workflow.

II. PACT Overview

The simulation flow of PACT (Fig.1) contains the following steps:

1) Users provide information about the chip stack, material properties, problem size, heat sink type, and cooling method to PACT.
2) PACT calculates each grid's lateral and vertical thermal resistance and capacitance, as well as determining the corresponding cooling parameters based on the selected cooling design.
3) PACT calculates and assigns values for resistance, capacitance, and power in circuits, then uses these values to create a thermal netlist.
4) Users can choose between transient or steady state simulation as well as among various differential equation solvers.
5) PACT utilizes OpenMPI [3] to enable parallel simulation.
6) PACT solves the RC thermal netlist using the SPICE engine of PACT and outputs the temperature traces along with the simulation time and resource usage summary. Currently, we use Xyce as the PACT SPICE engine.

Users can clone and use the default version of PACT[1] on their own systems. Also, we provide a containerized version in our PACT repository to enable easy adoption without having to install dependencies (i.e., Xyce SPICE simulator). In the containerized version, users can use Docker to build a new image (or use our latest released image) and run their simulations on it. In addition, we developed a simple visualization tool for PACT (VisualPACT) that provides thermal maps corresponding to the temperature dissipation during the simulation.

[1] https://github.com/peaclab/PACT

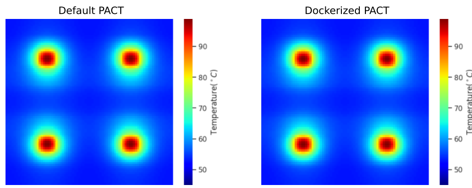

Fig. 2. VisualPACT output for default and containerized PACT.

III. PACT DESIGN AND IMPLEMENTATION

We next briefly discuss the key components of PACT.

A. Thermal netlist and SPICE circuit components

PACT calculates the thermal resistance, capacitance, and heat flow values. As a SPICE-based simulator, PACT leverages circuit components from the SPICE library to construct the thermal netlist. Users can enhance PACT by integrating additional libraries, and this flexibility allows PACT to adapt to emerging advancements in the field.

B. OpenRoad Interface

OpenROAD [4] is a comprehensive open-source RTL-to-GDS (Register-Transfer Level to Graphic Data System) flow. OpenROAD generates post-routing design exchange format (DEF) files describing a circuit's detailed placement and routing information [4]. OpenROAD's spatial power information at the standard-cell level can be fed into PACT. PACT uses the DEF files to generate the power values for each instance in the design using OpenSTA, which is a static timing analysis tool that supports gate-level simulation. In addition, PACT can be used as the backend thermal simulator for other commercial simulators (e.g., Cadence and Synopsis)

C. PACT Solver

Unlike other CTM-based simulators, PACT supports various steady-state (e.g., KLU, SuperLU, and AztecOO) and transient solvers (e.g., Trapezoidal, backward Euler, and Gear). These solvers enable PACT to solve thermal netlists across diverse chip architecture designs at varying simulation granularities.

IV. EXAMPLE USE CASE

To demonstate our new containerized version of PACT, we ran simulations using both default PACT and containerized PACT for a specific chip. In this experiment, test chip sizes are set to $5mm \times 5mm$, power traces are non-uniform, and there are multiple off-center hot spots. By using VisualPACT, we created temperature maps to demonstate the final result of both transient simulations (see Fig. 2).

We validated PACT's accuracy by comparing transient and steady-state simulation of PACT results with COMSOL, a FEM-based simulator. In our experiments, a comparison with COMSOL reveals that PACT exhibits maximum, average, and minimum grid temperature errors of 2.77%, 1.76%, and 0.89%, respectively [2]. This underscores the accuracy of PACT in

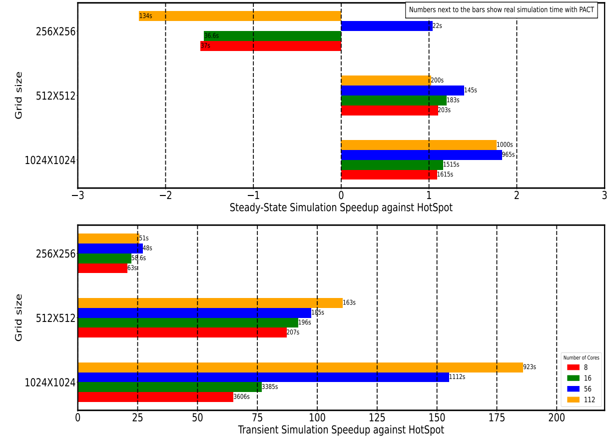

Fig. 3. Steady-state and transient speedup of PACT against HotSpot. Steady-state and transient solvers used in PACT in this experiment are AztecOO and TRAP, respectively.

achieving steady-state simulations. For transient simulation, when contrasted with COMSOL, PACT exhibits a maximum and average difference of 3.28% and 1.1%, respectively.

As PACT is a parallel thermal simulator, we compare the simulation speed of PACT to HotSpot using parallel simulation mode with different numbers of cores. We used OpenROAD benchmark circuits to show the speedup of PACT's simulation time against HotSpot in Fig.3. Negative values in Fig.3 show PACT is slightly slower than HotSpot for very short simulation times, mostly owing to HotSpot being written in C/C++ (versus PACT front-end written in Python). The maximum steady-state speedup compared to HotSpot is $1.83\times$. Figure 3 illustrates that PACT achieves significant running time reduction compared to HotSpot in every transient test case. In fact, PACT achieves a speedup of up to 186× when compared to HotSpot.

V. LIMITATION AND FUTURE WORK

The present iteration of PACT exclusively accommodates cuboid grids. Alternative grid shapes, like circular ones (particularly beneficial for simulating round heat pipes), can only be approximated using multiple cuboid grids. Furthermore, the existing iteration of PACT lacks support for an adaptive (non-uniform grid) grid. Also, PACT does not account for quantum effects at the nanometer scale (40-300 nm).

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