Morning Program

9:00-10:00

Keynote: “Pitfalls in Architecting an Autonomic Power Controller”

Speaker: Pradip Bose – IBM T. J. Watson Research Center

Abstract: Modern processor systems are equipped with on-chip or on-board power controllers. Dynamic power and temperature management algorithms have been pursued extensively in the research literature, and some of the most promising ones are finding themselves incorporated in suitably adapted forms in power management firmware. In this talk, we examine the pitfalls in architecting such dynamic power management control systems at the chip or system level. A key question that we pose is: How to ensure that such managed systems are "energy-secure?" In other words, what are the challenges in verifying that the system will always meet the energy-related behavioral specifications? And, how to make sure that the algorithms implemented cannot be exploited to make the system unstable or unreliable by launching a malicious virus program? What intelligent safeguards must future dynamically managed systems possess to ensure that such security holes do not exist? We will discuss new advances in intelligent, energy-secure system architecture research starting with measurement and modeling based assessment of potential vulnerabilities in current generation systems.

Speaker Bio: Pradip Bose is a Research Staff Member and Manager at IBM T. J. Watson Research Center. The current area of focus for his department is power-efficient, reliable microprocessor systems. Pradip holds a Ph.D in electrical & computer engineering from University of Illinois at Urbana-Champaign. He has been with IBM Research for over 28 years. He has been involved in the definition and modeling of the whole line of POWER-series microprocessors at IBM, beginning with the first RISC super scalar processor, code-named Cheetah (later America) that led to the original RS/6000 offering. He is an IBM Master Inventor and a member of the IBM Academy of Technology, and has received several innovation and accomplishment awards from IBM. He is a Fellow of IEEE.

10:00-10:25

“Adaptive Energy Management for Enterprise Server Workloads”

Speaker: Karthik Kumar – Intel Corp.

Authors: Martin Dimitrov – Intel Corp.
          Kshitij Doshi – Intel Corp.
          Karthik Kumar – Intel Corp.

Abstract: Increasing power and cooling costs for data centers has brought about a sharp focus on power management for enterprise servers. The vast diversity in enterprise workloads and their behavior makes it difficult for hardware to leverage power-saving mechanisms without including feedback from the
An analysis of component-wise power breakdown in an enterprise server shows that the two largest consumers of power are the memory and processor systems, which together may typically account for more than 70% of the total power consumption. In this talk, I describe some initiatives undertaken by our team, targeted at workload based energy management for these systems. The talk is organized in two parts. In the first part, I describe some of our efforts in adapting memory configurations based on workload behavior. I describe a scheme to adapt the row buffer management policy based on power and performance considerations. I also analyze the impact of adapting memory frequency, capacity, and bandwidth. In the second part, I describe a tool to adaptively reduce processor power consumption using workload behavior. We show some of our preliminary results, and describe some opportunities for future work.

10:30~11:00 Morning Break

11:00-11:25
“Minimizing Thermal Variations in Liquid-Cooled 3D MPSoCs Through Cavity Modulation”

**Speaker:** Mohamed Sabry – EPFL

**Authors:** Mohamed Sabry – EPFL
David Atienza – EPFL

**Abstract:** Inter-tier liquid cooling is a recently proposed methodology that effectively reduces the increased temperatures in 3D multiprocessor system-on-chip (3DMPSoC). However, due to the heterogeneous power dissipation map of the functional modules, liquid cooling has a significant impact on augmenting the thermal variation within a single tier. In this presentation, we first propose a novel approach to minimize the thermal gradient of 3D MPSoCs with liquid cooling via cavity modulation, where we can vary the structure of the etched cavity tier to meet the cooling demands required by each computing element. We formulate the structure variation problem as an optimal control problem to minimize the thermal gradient in each functional block with negligible manufacturing cost, which can then we combined with dynamic thermal management to reduce overall the thermal gradient of 3D MPSoCs below 5% at run-time without wasting energy in the cooling infrastructure. As a second proposal in this work, we describe a new family of global hardware/software temperature controllers based on fuzzy logic for energy-efficient 3D MPSoC cooling. These novel controllers include a thermal-aware job scheduler, which balances the temperature across the system to maximize cooling efficiency. Furthermore, this new generation of system-level temperature balancing controllers forecast maximum system temperature, and uses this forecast to proactively set the liquid flow rate. Hence, the proposed controller avoids over- or under-cooling due to delays in reacting to temperature changes. The experiments on modeled 2- and 4-layered 3D MPSoCs show that the proposed global cooling controller prevents the system to exceed the given threshold temperature while reducing cooling energy by up to 85% and system-level energy by up to 40% in comparison to using a static worst-case flow rate setting in datacenter servers. Moreover, our current results show that temperature-aware load balancing reduces hot spots and gradients significantly better than state-of-the-art load balancing or reactive thread migration without temperature considerations in forthcoming 3D MPSoCs, thus enabling up to 60% energy savings with respect to state-of-the-art datacenter server designs.
“Runtime Task Allocation Techniques for QoS and Energy Sensitive Control of Aging-rate in Embedded Multithreaded Dataflow Applications”

Speaker: Andrea Acquaviva – Politecnico di Torino

Authors: Andrea Acquaviva – Politecnico di Torino
Francesco Paterna – University of Bologna
Luca Benini – University of Bologna

Abstract: Due to the aggressive technology scaling and the increasing utilization imposed by multimedia workloads, lifetime preservation is becoming one of the most relevant issues in Multiprocessor System-on-Chip (MPSoC). However, lifetime and energy conservation are often contrasting objectives. As lifetime is a function of components utilization, a viable solution to achieve a desired lifetime versus energy/performance trade-off is to exploit the degrees of freedom available in a MPSoC concerning the allocation of multimedia tasks on processing cores. However, policies must be developed in order to hide as much as possible the impact on QoS and energy during application execution and the perceived usability of the platform across its whole lifetime. In this talk, runtime adaptive task allocation techniques are presented, which exploit a wear-out prediction model to improve chip lifetime in a energy sensitive way. Their evaluation on a parallel implementation of a MPEG2 decoder ported on a multi-core virtual platform is discussed.

12:00~1:30 Lunch Break

Afternoon Program

1:30-2:30

Keynote: “Sustainable IT Ecosystem: Enabled by Resource Supply and Demand Management”

Speaker: Zhikui Wang – Hewlett-Packard Co.

Abstract: The IT industry is found responsible for about 2% of global greenhouse gas emissions. The challenges for the industry are to reduce the IT footprint significantly, while playing a critical role in addressing the global sustainability issue. An end-to-end perspective and a systemic approach are critical to address the sustainability of the IT ecosystem that is made up of billions of service oriented devices and thousands of data centers. In this talk, we present a supply-demand management framework for design and operation of the data centers that are the cores of the IT ecosystem. The framework, demonstrated at scales, integrates the techniques and tools for lifecycle analysis and design, pervasive sensing and communication, knowledge discovery and visualization, and autonomous control and optimization. We also discuss our vision on how the framework can be extended for resource management through the IT ecosystem at the scale of urban infrastructures.

Speaker Bio: Zhikui Wang is a senior research scientist in HP Labs, Hewlett-Packard Company, located in Palo Alto, California. He joined HP Labs in 2005 after he received his Ph.D. degree from University of California, Los Angeles in Electrical Engineering (Control Systems). He received his Master of Engineering degree in Industrial Automation from Chinese Academy of Sciences in 1998, and Bachelor of Engineering degree in Process Automation and Automatic Instrumentation from Tsinghua University.
in 1995, both in Beijing, China. His research interests are in application of control and optimization techniques in sustainable ecosystems, including application performance control, workload management, data center power management and cooling control.

2:30-2:55

“Hierarchical Power Management for Adaptive Tightly-Coupled Processor Arrays”

**Speaker:** Vahid Lari – University of Erlangen-Nuremberg

**Authors:**
- Vahid Lari – University of Erlangen-Nuremberg
- Srinivas Boppu – University of Erlangen-Nuremberg
- Shravan Muddasani – University of Erlangen-Nuremberg
- Frank Hannig – University of Erlangen-Nuremberg
- Jürgen Teich – University of Erlangen-Nuremberg

**Abstract:** This paper presents techniques for self-adaptive hierarchical power management for parallel processor array architectures supporting a new resource-aware parallel computing paradigm called invasive computing. Here, an application may dynamically claim for resources in three phases of execution: resource acquisition (invade), program loading/configuration and execution (infect), and release (retreat). Resource invasion is controlled by proper controllers called ICPs and integrated into each processing element (PE), and several invasion strategies such as for claiming linearly connected as well as rectangular regions of PEs have been implemented currently. Here, we investigate the key idea of an application-driven hierarchical power management by allowing the applications themselves to control the power for PE and ICP domains hierarchically during their execution. Whereas each PE is assigned a separate power domain, the grouping of invasion controllers (ICPs) into different power domains as well as other design options are explored so to tradeoff power, area, and performance.

2:55-3:20

“Power Management Made Simple, But Not Simpler: A Control-theoretic Perspective”

**Speaker:** Paul Bogdan – Carnegie Mellon University

**Authors:**
- Paul Bogdan – Carnegie Mellon University
- Radu Marculescu – Carnegie Mellon University

**Abstract:** Shrinking transistors sizes has led not only to increasing computational power and so the emergence of Networks-on-Chip paradigm, but also to higher power consumption. To overcome the power barrier in future multicore platforms, it is necessary to enhance the NoC designs with dynamic algorithms that allow the scaling of supply voltage and frequency as a function of the workload characteristics and parameter variations. Consequently, in this talk, we discuss advanced feedback control mechanisms that can dynamically adjust the operating frequencies of an NoC consisting of multiple voltage and frequency islands (VFIs). To surpass the challenges of centralized control algorithms, we also review a small world inspired approach to control the operating frequencies of various VFIs while minimizing the power consumption and satisfying predefined performance constraints. Such an approach changes dramatically the traditional design and, at the same time, enables the use of adaptiveness as a mean to compensate for workload and process variability fluctuations.
“Accurate Online Power Estimation and Automatic Battery Behavior Based Power Model Generation for Smartphones”

Speaker: Lide Zhang – University of Michigan
Authors: Lide Zhang – University of Michigan
Robert Dick – University of Michigan

Abstract: This work describes PowerBooter, an automated power model construction technique that uses built-in battery voltage sensors and knowledge of battery discharge behavior to monitor power consumption while explicitly controlling the power management and activity states of individual components. It requires no external measurement equipment and requires no manual measurement or data processing. We also describe PowerTutor, a component power management and activity state introspection based system that uses the model generated by PowerBooter for online power estimation. PowerBooter is intended to make it quick and easy for application developers and end users to generate power models for new smartphone variants, which each have different power consumption properties and therefore require different power models. PowerTutor is intended to ease the design and selection of power efficient software for embedded systems. Combined, PowerBooter and PowerTutor have the goal of opening power modeling and analysis to the masses – of both smartphone variants and their users. They have taken first steps in that direction, with PowerTutor logging use by over 3,750 individuals. PowerBooter and PowerTutor presently support Google Android handsets and are being ported to other hardware–software platforms.

“Adaptive Control of Voltage- and Current-Mode Regulators for Photovoltaic Module Emulators”

Speaker: Naehyuck Chang – Seoul National University
Authors: Younghyun Kim – Seoul National University
Naehyuck Chang – Seoul National University
Massoud Pedram – University of Southern California

Abstract: Solar energy is environmentally friendly, and is gaining tremendous interest as one of the most practical sustainable energy sources. Solar-powered systems mandate joint optimization of the photovoltaic (PV) module and the load device, which requires elaborate experimental setup and extensive experimentation. PV (module) emulators, which can provide reproducible and controllable input power profile for a load device corresponding to different ambient conditions for a PV module, can significantly reduce the level of effort and cost for the development and optimization of the PV module servicing the load device.

In this paper, we describe a dual-mode power regulator for PV emulation. The dual-mode regulator consists of a voltage regulator and a current regulator, connected by two diodes for power hybridization. The circuit switches between the two regulators in order to accurately emulate the electrical output behavior of a PV module under different ambient conditions (e.g., solar irradiance, temperature) and load...
demands. The proposed regulator circuit provides accurate emulation results over the full operating range of the PV module by complementary use of the two regulators. Measured results show 1-3 of output variations by 20% of load power variation when using appropriate power sources, compared with 13-15 otherwise. We develop a robust control method for producing an accurate I-V curve with compensation of the loss in the circuit components. We validate the behavior of the proposed circuit and control method by Matlab/Simulink simulations and experiments.

4:35-5:00

“Power Distribution in Locally Daisy-Chained Sensing Systems”

Speaker: Sehwan Kim – University of California, Irvine
Authors: Sehwan Kim – University of California, Irvine
Pai H. Chou – University of California, Irvine

Abstract: This paper proposes a method for saving power in locally daisy-chained sensing systems. Such a system consists of a data aggregator with a data uplink and distributes power to one or more daisy-chained nodes that perform sensing and transmit the data back to the data aggregator. We reduce power consumption at two levels. First, instead of keeping the power lines on for the entire time, we transmit power at a higher voltage to increase the efficiency of power delivery. Second, we add supercapacitors to the sensing nodes so that they can be charged quickly during sleep mode and power the nodes when the peak current is required by the active mode, as well as most time of sleep mode, thereby minimizing transmission loss. The data aggregator can even go into power-down mode and be waken up by sensing nodes upon event detection by varying the power lines voltage. Experimental results show that our proposed techniques significantly reduce power consumption.