Fabrication of freely suspended nanostructures by nanoimprint lithography

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We describe an innovative approach to fabricate freely suspended nanometer-scale structures. In this approach based on nanoimprint lithography, the imprint polymer serves as both the *pattern mask* and the *sacrificial layer*. The fabrication involves imprinting the pattern to be suspended upon an existing structure, metallizing the pattern, and removing the excess material. To demonstrate the basics, we have fabricated families of suspended beams. This approach potentially possesses all the desirable aspects of nanoimprint lithography and is suitable for use in simple layer-by-layer fabrication. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2180872]

Nanoimprint lithography (NIL) is a high volume, low cost patterning technique with spatial resolution down to ~5 nm.[1] In basic NIL, a pattern is defined by physically deforming a polymer resist. One typically uses a solid template as the imprint mold, which is prepared by electron beam lithography (EBL) and reactive ion etching (RIE).[2] The mold is pressed upon a polymer-coated substrate, deforms the polymer at elevated temperature, and is removed from the substrate after cooldown. The pattern imprinted on the polymer can then be transferred into the substrate by a variety of techniques. In the past decade, NIL has been used to fabricate electronic,[3] photonic,[4] and microfluidic[5] devices.

In this paper, our focus is on extending the NIL technique to the fabrication of freely suspended nanostructures. Such suspended nanometer-scale structures are finding considerable use in emerging semiconductor devices. Nanoelectromechanical systems (NEMS),[6] for instance, are mostly realized as freely suspended doubly clamped or cantilevered beams. Similarly, three-dimensional photonic band-gap materials[7] can be manufactured in the form of a matrix of suspended dielectric or metallic nanostructures. For the fabrication of these experimental devices, researchers have, for the most part, combined EBL with subtractive fabrication techniques.

It is challenging to fabricate next generation semiconductor devices with suspended nanostructures by EBL-based approaches. First, EBL makes high volume fabrication challenging. Second, subtractive techniques quickly become complicated for manufacturing suspended structures with more than one layer. Here we describe an alternative, NIL-based approach to fabricate suspended nanostructures. The presented approach potentially possesses all the desirable aspects of NIL; it also lends itself to simple layer-by-layer fabrication. With this approach, one can generate suspended nanostructures upon an existing structure, such as anchors, without modifying the structure—given that the polymer patterning resist serves as the sacrificial layer.

We now turn to a detailed description of the NIL-based fabrication approach. The device fabricated in this preliminary work contained two layers: an anchor layer and a freely suspended layer. The anchor structure was made up of SiO_2 and Al, and was fabricated by conventional nanoimprint and film deposition steps. Figure 1(a) shows a scanning electron microscope (SEM) image of the anchors on the sample chip. After the fabrication of the anchors, we spin coated a thick polymer layer upon the chip for the second layer imprint. We used poly(methyl-methacrylate) (PMMA) 950KA3 (3% in anisole) as our polymer. The thickness of the PMMA after coating several layers was ~2 μm. As such, the PMMA was

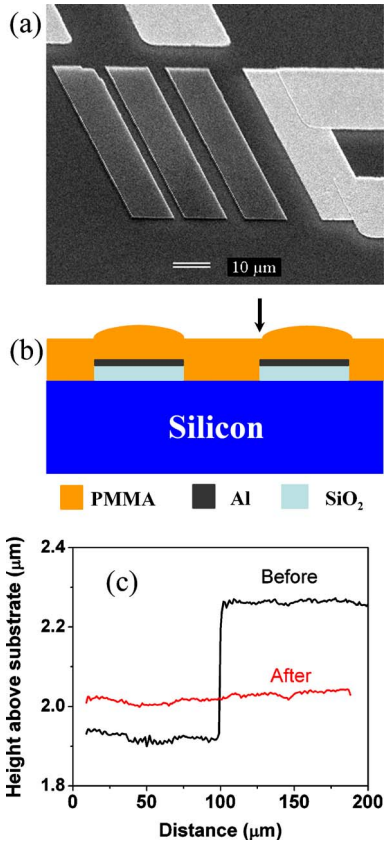

FIG. 1. (Color online) (a) Scanning electron microscope (SEM) image of the anchor structures. These are rectangular structures with $l \times w = 70$ μm $\times 12$ μm. The height is 300 nm. (b) An illustration of the sample chip after it is spin coated with PMMA. (c) The height profile data across the anchor [arrow position in (b)] before and after flattening.

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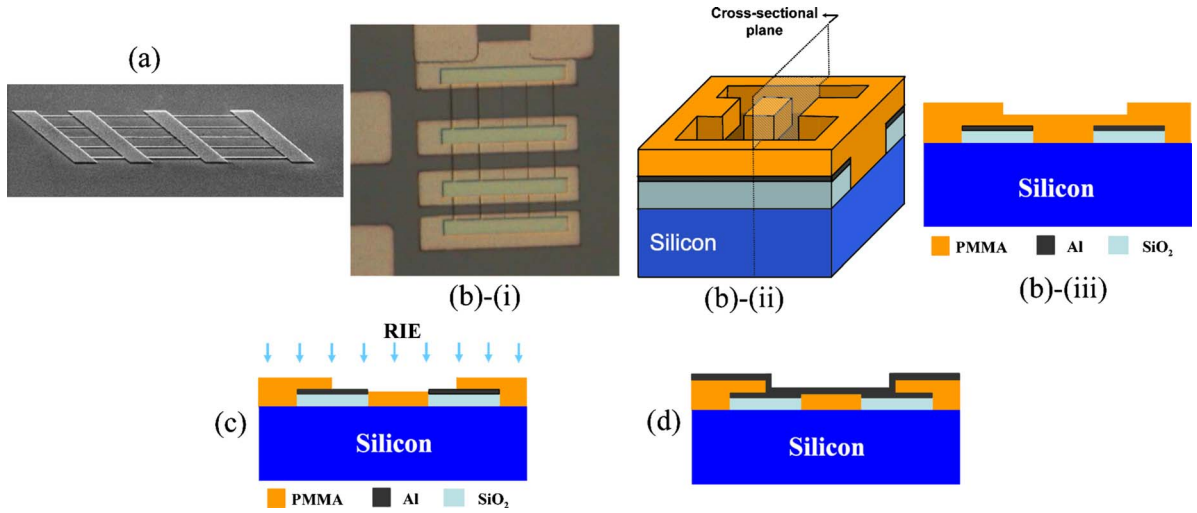

FIG. 2. (Color online) (a) SEM image of the imprint mold for the second layer. The beam structures in the mold have the following lengths, l, and widths, $w:l=10$, 12, and 15 μm; $w=1$ μm, 500 nm, 250 nm, 120 nm, and 80 nm. The height of the structures is $t=300$ nm. Note that the beams are longer than the separation between the anchors shown in Fig. 1(a). (b) (i) Optical microscope image of the second layer imprint upon the anchor structures. The cross-sectional illustration in (iii) is through the position of the dotted line in (ii). (c) Removal of the residual PMMA using O_2 RIE. (d) Thermal deposition of Al upon the patterned sample chip.

thick enough to cover the anchor layer and allowed enough room for the second layer imprint.

One important issue that we needed to deal with was the flatness of the spin-coated PMMA. The PMMA coating was not flat even after a very thick coating layer—as shown in Fig. 1(b). In order to flatten the PMMA, we used an extra imprint step using a planar mold.[8] Figure 1(c) shows the profile of the ~2-μm-thick PMMA upon the anchors *before* and *after* this step. Initially, the height profile of the PMMA matched almost identically to the anchor profile. After the imprint, the PMMA was flat.

The Si mold for the upper layer was fabricated by EBL and RIE. The structure was subsequently coated with an antiadhesion layer. The completed mold is shown in Fig. 2(a). It has several nanoscale beams with varying length, l, and width, $w:l=10$, 12, and 15 μm; $w=1$ μm, 500 nm, 250 nm, 120 nm, and 80 nm. The height of the structures was $t=300$ nm.

The imprint process was performed in a flip-chip bonder.[9] One important aspect of imprinting the second layer upon the anchors was the alignment between layers. The sample stage of the bonder had a 100-nm motion step; a 400× microscope was used to monitor the alignment[10] as the sample stage was moved in stepwise fashion. In this initial work, our structures did not require high alignment accuracy. In order to avoid the adverse effects of thermal expansion, the alignment was performed at the elevated imprint temperature of $T=180$ °C. At this temperature, an imprint pressure $P=130$ bar was used for a period of 6 min. Before separating the mold and the sample chip, the system was cooled to 85 °C by flowing N_2. The optical micrograph of the resist after the imprint and an illustration of the structural layers on the sample chip are shown in Fig. 2(b).

We used a carefully timed O_2 RIE to remove the residual PMMA upon the anchors. For this etch step, we used an O_2 flow rate of 8 sccm (standard cubic centimeters per minute at STP) at a background pressure of 100 mTorr and a rf power of 100 W resulting in an etch rate of ~8 nm/s. Once the anchor structures were completely exposed, we thermally deposited a 200-nm-thick aluminum film as the device layer. Figures 2(c) and 2(d) illustrate the removal of the residual PMMA and the thermal deposition steps.

Ideally, at this point in the fabrication process, a simple lift-off step in a solvent such as acetone would result in the release of the suspended nanostructures. In our experience, however, lift-off did *not* work reliably. This is partly due to the fact that the imprint pattern does *not* have an *undercut*, and the deposited film is essentially connected over the entire sample area.[11] Immersing the sample in an ultrasonic bath was also prohibitive due to the fragile nature of the suspended nanostructures. In order to overcome this challenge, we used a process similar to the wet etch step common in standard semiconductor processing.[12] This improved etch step can be regarded as a *device-protected-etch*, and is illus-

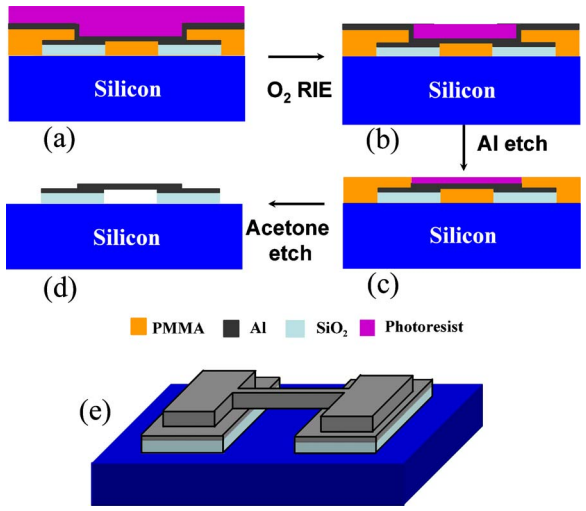

FIG. 3. (Color online) Illustration of the device-protected-etch process, (a) First the sample is spin coated with photoresist S1813. (b) After a carefully timed O_2 RIE to etch the photoresist, the elevated Al layer is exposed. Note that the area of the sample chip where the nanostructures are located is still covered with the photoresist. (c) Al is removed, but the nanostructures are protected. (d) Using acetone, the PMMA is dissolved and the nanostructures are released. (e) Oblique view of the finished structures showing the beams crosscutting the anchors.

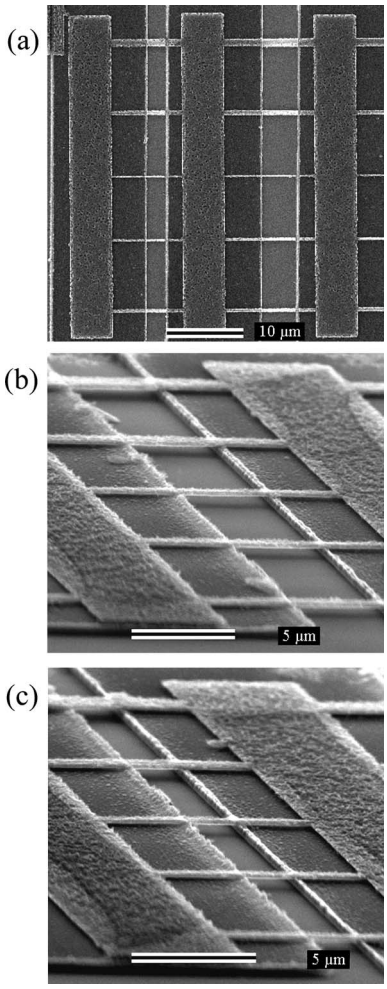

FIG. 4. SEM images of the finished suspended nanostructures. (a) Top view showing two families of beams with suspended lengths $l=5$ μm and $l=3$ μm. The widths in each family vary as (top to bottom) $w=1$ μm, 500 nm, 90 nm, 120 nm, and 250 nm. (b) Side view of 5-μm-long beams. (c) Side view of 3-μm-long beams.

trated in Fig. 3. The basic idea is to generate a relatively flat protective coating over the whole sample chip and etch downwards until one reaches the elevated, excess metal area. Note that there will still be protective coating on the device area due to the height profile [see Fig. 3(c)]. In this work, we chose microposit S1813 photoresist as the protective coating. We spin coated the sample with S1813 at 2000 rpm for 65 s, followed by soft and hard bake steps. Due to the viscosity and the reflow during the bake, the surface of the S1813 was flat. The coated sample was then etched in a RIE chamber using O_2 at a flow rate of 10 sccm and a background pressure of 200 mTorr, and a rf power of 150 W. The etching rate under these conditions was ~6 nm/s. We stopped etching when we reached the elevated Al film surface; we then used a wet aluminum etchant to remove the Al. As expected, the devices survived under the protective S1813 coatings. The final step in the fabrication was the release of the nanostructures in acetone.

The electron micrographs of the fabricated devices are displayed in Fig. 4. Both top [Fig. 4(a)] and side views [Figs. 4(b) and 4(c)] show suspended Al beams of two lengths, $l=5$ μm and $l=3$ μm. The widths of the beams are in the range 90 nm$<w<1$ μm, which is consistent with the dimensions in the mold [see Fig. 2(a)]. The apparent roughness on the suspended Al layer is possibly due to the parameters used during the thermal deposition. We believe that the roughness at the edges of the anchor pattern could be due to the residual stress in the SiO_2. We also note that, in some longer and less stiff beams (not shown), the surface tension forces of the liquid after the PMMA removal in acetone resulted in the collapse of the structures. In such instances, it would be desirable to use a dry etch to remove the sacrificial layer, i.e., the PMMA.

The approach described here potentially possesses all the desirable aspects of NIL. The feature size and the resolution (pitch) in the upper layer could possibly be extended down to ~10 nm. The broadening observed in the size of our smallest beams is due to the fact that we used a thick Al structural film; this should be avoidable by depositing thinner films. It should also be possible to extend our approach to the fabrication of multilayered structures. In such a task, after finishing the fabrication of a given layer, one would coat the sample chip with PMMA again, flatten the PMMA, align to the layer below and imprint the new layer. After material deposition, and the removal of excesses, one would end up with a new layer. By repeating this formula, it would be possible to generate devices with multilayers in a layer-by-layer fashion.

In summary, we have demonstrated the fabrication of freely suspended nanoscale structures using NIL. Our approach may find use in the fabrication of a variety of devices including NEMS and photonic band-gap materials.

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