EC527: High Performance Programming with Multicore and GPUs -- Spring, 2018

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TFs: There is no TF. Help in this course is limited to helping solve system problems.

Mission Statement: “Programming for performance using the capabilities of modern processors”

Course Description (catalog): Considers theory and practice of hardware-aware programming. Key theme is obtaining a significant fraction of a program’s potential performance through knowledge of the underlying computing platform and how the platform interacts with programs. Studies architecture of, and programming methods for, contemporary high-performance processors. These include complex processor cores, multicore CPUs, and graphics processors (GPUs). Labs include use and evaluation of programming methods on these processors through applications such as matrix algebra and the Fast Fourier Transform.

Prerequisites: Computer Organization (EC413 or equivalent), programming in C, and academic maturity sufficient, e.g., to learn new programming tools from professional documentation and to design basic experiments and perform simple data analysis.

Course Motivation:
For several decades programmers found the von Neumann (vN) model to be an adequate worldview for obtaining most of the potential performance from target systems. This model is familiar: instructions are executed serially in a single stream and data are stored in a single image of memory. Instruction executions and memory accesses are assumed to be uniform. Except for specialized processors--DSPs, Supercomputers, MPPs--good vN programming plus a good compiler meant taking advantage of most of a computer’s capability.

Recent directions in processor architecture—complex memory hierarchies with many layers of cache, superscalar and deeply pipelined CPUs, multicore, and accelerators such as AVX, GPUs, and FPGAs—have made the vN approach to obtaining performance obsolete. For many applications performance is secondary; in those cases current methods remain appropriate. But for applications requiring performance, a deeper level of machine understanding is required: the programmer must be aware of the underlying hardware at all stages of software development from algorithm selection and numerical analysis, through coding, to interaction with system tools such as compilers and libraries, and finally debug, tuning, optimization, and maintenance.

Texts and Organization (supplemented with additional articles, lecture notes, and tutorials):
For complete (tentative) readings see “Readings” document.

Part 0 – Methods
• Timing and Timers – See Lab 0 documentation
• Performance Models – Patterson & Hennessy 5e, Chapter 6.1, 6.2, 6.10, 6.11

Part 1 – Single core
This part of the course is based on sections of courses taught at CMU and ETH.
• “How to Write Fast Code,” Markus Pueschel, Lecture Notes from CMU and ETH
• Computer Systems: A Programmer’s Perspective, Bryant & O’Hallaron, Chapters 5 and parts of Chapter 6
• Various Intel HW & SW Reference Manuals
Course Mechanics

- **Style:** One of the missions of this course is to be a practicum associated with the computer organization and architecture curriculum. As such we explore contemporary high-end processors in some depth and then practice using that knowledge to obtain high resource utilization with real programs. The emphasis is therefore on programming with lectures in support of the labs. Lectures will also introduce appropriate theory when necessary, especially with respect to performance evaluation.

- **Grading:**
  - Exam(s): 35%
  - Programming/Homework Assignments: 40%
  - Final Project: 25%

Please note that these percentages are tentative. Also, that the impact of an assignment/exam grade on the final grade depends on the variance in addition to the percentage.

- **Weekly Assignments:** Until the beginning of the project there will be weekly assignments, 10 in all (0-9). All involve programming, mostly exploring small amounts of code in great depth. Some assignments involve pencil-and-paper problems in addition to programming.

- **Late Policy:** Assignments must be submitted on time, usually on Mondays before class. There is a 20% per day penalty. You will get a total of 5 “free” late days to handle special (but common) occurrences such as illness, interviews, etc. Otherwise the only acceptable excuses will be “uncommon” events such as long term disability, family crisis, etc.

- **Academic Honesty versus Collaboration:** You are encouraged to work together to learn the material and to discuss approaches to solving problems. However, you must come up with and write up the programs and other solutions on your own.

- **Exams:** There will be at least one mid-term exam. There may also be a final exam.

- **Final Project:** The purpose is to add depth and to practice the concepts learned in an extended case study. Results will be written up conference paper style and presented to the class. You may work in teams of up to three students. This year I will try to get an early start on the project and integrate it into the assignments.

- **“Late” Classes:** Unfortunately, this class has been scheduled so that it sometimes conflicts with distinguished lecture speakers. Therefore, on at least 2 days, class will be from 5:00-6:45. There may be a few more shifts -- these will be announced well in advance.
Course Objectives

Review
• Computer architecture including memory hierarchy and basic pipelining.

Learn about
• Various contemporary high-end processors, in particular the latest Intel cores and memory hierarchy, multicore cache, and GPUs
• Methods of performance evaluation
• Methods of hardware-aware code development
• How to program complex hardware to obtain high utilization

Gain experience with developing efficient programs, including
• using extended instruction sets (AVX) with implicit code and intrinsics
• synchronization
• methods of parallel programming, including PThreads and OpenMP
• cache-aware optimizations
• CUDA for GPU programming

From the Course Requisition Form

Basic Goals
1. Students should learn enough about processor architecture and programming to write fast code (code with high utilization of available resources) on contemporary processors.
2. The knowledge and experience should enable students to extend this capability to new processors and to large and varied applications.

Detailed Goals
Students should have a good understanding of theory and practice of
1. Measuring and analyzing performance
2. Developing fast code using methods such as decomposition, mapping, load balancing, blocking, basic block optimizations, and many others
3. Using advanced capabilities such as SIMD vector extensions and use of intrinsics
4. Parallel processing with small-scale (multicore) shared memory processors with both PThreads and OpenMP
5. Programming GPUs, including dealing with the standard inhibitors to getting good performance
Students should also develop a deeper understanding of one of the three technologies (CPU, multicore, GPU) with an extended project. This will consist of examining a more complex numerical or data processing problem.

Course Outcomes
1. Sufficient knowledge of various processor architectures to be able to write high-performance programs
2. Basic knowledge of principles and practice of performance evaluation and writing high-performance programs with the goal of applying this knowledge to other processors.
3. Ability to use AVX instructions set extensions
4. Ability to write parallel programs using PThreads and OpenMP
5. Ability to write GPU programs in CUDA
6. Ability to formulate and design programs at a high level accounting for a target architecture