VLSI EC571
Fall 2017

Course Number: EC 571    Course Name: VLSI Principles & Applications    Semester: Fall 2017
Number of credits: 4    Prerequisites: EC 311 (Intro to Digital Logic), EC 410 (helpful but optional)    Lecture time & place. STH 113
Labs are at-will (not scheduled, I will get you all the access you need)

Available materials and links. See LEARN

Staff Information
Instructor:
Name: Allyn E Hubbard
Office address: Room no: 329 PHO
Office phone number: 617-353-2815
You may call me (if it’s urgent) on my cell 508 561 5320 and leave a message. I often do not pick up numbers (robots) that I do not recognize. EMAIL IS BEST.

E-mail address: aeh@bu.edu
URL: www.bu.edu/vnns

Office hours: 4-7 TTr Otherwise at any time, stop in if my door is open, and I will see what I can do for you. Generally these walk-in visits should be “real short” so I can take care of it simply, or “real important” and I’ll help you right away or schedule a time, and the time allowed can be unlimited.

Lab Hours: You have “class access” to the lab (Pho 305), which means you can go anytime the lab is scheduled to be open. We are in the process of changing to a new system with an actual lab text manual. You will find it useful in general, but it was not written specifically for our system at BU, so the paths are not relevant. The tutorial will take you through everything, so in general you do not need to know much about paths, especially setup paths. You will need to keep track of your own subdirectories, as is the normal situation.

Course Resources

Textbooks:

Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Erik Brunvand. Addison-Wesley (This is a lab book). Given the new tutorials, this book is probably not necessary.
References (usually done through “learn”)

Notes:

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**Evaluation**

**Grading criterion:** Two tests and a final @ 20% each. Labs 35%. Homework 5%.

**Homework:** See schedule on LEARN.

**Quizzes:** In class.

**Midterm exams:** The exams are scheduled in the “course schedule” on CourseInfo.

**Final exam:** 20%. See University schedule

**Lab work:** You may collaborate, but **eventually produce individual work.**

This rule may be superseded in cases that the professor requests that you work on separate parts individually, and assemble them as in the case of a project. Such cases will be clearly defined, so don’t assume that the project policy is in effect normally.

Reports, class participation, etc.: IT COUNTS!!! Make yourself a participant!

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**Course objectives**

By the end of the course, you should be able to design a CMOS circuit that performs some arbitrary logical or system function to an arbitrary performance specification.

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**Course schedule:** For a detailed schedule of lectures, labs, homeworks, etc: See the “Schedule with labs and homeworks” file in LEARN. The course schedule may change as the lab materializes, but the changes should not be substantial. I don’t expect any snow days during the fall semester.

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**Policy**

Absences (from lectures, labs, etc.), missed work, make-up exams, etc.

**Late work:** Labs lose 5% per day after the due date down to a maximum of 50%. Example: A lab is >10 days overdue, the maximum attainable grade will be 50 rather than 100.

I and W grades: As per University policy.

**Collaboration on different types of assignments:** You may collaborate but **eventually hand in individual work.** This rule may be superseded in cases that the professor requests that you work on separate parts individually, and assemble them as in the case of a project. Such cases will be clearly defined, so don’t assume that the project policy is in effect all the time.