EC311 - Introduction to Logic Design
Spring 2017
A1: MW 12:20 – 2:05pm in PHO 210
A2: T Th 1:30 – 3:15pm in PHO 202

Staff Information
Instructors:
  Tali Moreshet, PHO 528  Office hours: M 2-4, Th 3:30-4:30  Email: talim@bu.edu
  David Starobinski, PHO 431  Office hours: M 3-4, F 9-10  Email: staro@bu.edu

GTAs:
  Yijia Zhang, zhangyj@bu.edu  Office hours: Fri 4-6pm
  Shreeya Khadka, skhadka@bu.edu  Office hours: Thur 4:30-6:30pm

Lab assistants/ Graders:
  Ayako (Aya) Shimizu, shimizu@bu.edu, Shuxian (Chloe) Zhang, sxzhang@bu.edu
  Nicholas Arnold, nicka97@bu.edu, Benjamin Brown, byb@bu.edu
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Course objectives
The class covers the theory and practice of digital hardware design. Students will learn to formulate real world tasks using Boolean algebra and FSM theory, and to apply manual and computer-aided techniques to solve the problems. In addition, they will also learn fundamental circuit design and verification skills using Verilog HDL and FPGAs.

Textbooks

Assignments, announcements, course material, updated schedule, and other useful links will be posted on Blackboard (http://learn.bu.edu).

Goals
To provide students with:
  • An understanding of the basic tools of logic design
  • An understanding of sound design methodologies
  • An experience with hardware implementation and the use of CAD tools

Course Outcomes
As an outcome of completing this course, students should be able to:
  • Understand the applications of logic design
  • Understand abstraction and hierarchy in digital design
  • Understand what components are available for logic design
  • Understand the use of Boolean algebra in logic analysis and design
  • Understand logic minimization criteria and methods for use in design
  • Understand the concept of state in digital systems
  • Design combinational digital logic systems given specifications
• Design sequential digital logic systems (finite state machines) given specifications
• Implement logic designs in hardware and with CAD tools
• Discover component availability and data using the Internet or other resources

Evaluation
Grading: Three exams: 70%, Labs: 15%, Lab attendance: 5%, Homework: 10%.

Homework: Homework assignments will be posted on the Blackboard website on Thursdays. Homeworks are to be submitted on Blackboard before the specified deadline (the following Friday by 8pm). Submissions may be typed or scanned, as long as they are legible. No credit will be given for late homework, but the homework with the lowest grade will be dropped.

Labs: Lab assignments will be posted on the Blackboard website. Grades will be assigned by demonstrating the lab individually, and submitting the Verilog code on Blackboard. Students are expected to attend their scheduled lab section every week.

Exams: The first two exams will be during class time. The third exam will take place during the scheduled final exam timeslot.

Course Policies
• Exam/Home/Lab Grade discussion: Grade discussion/corrections should be done within one week after the graded exam or homework is distributed. No grade changes will be made after one week.
• Academic integrity:
  o The homework and lab assignments must be the result of your individual work. You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and write the solutions of HW/Lab problems by yourself. Copying the solution and/or answer from another student or source is considered cheating.
  o Clearly reference any sources you used in your work: books, Internet, and your collaborators!
  o Boston University’s academic code of conduct will be strictly applied.
  o Boston University’s computing ethics will be strictly applied.