EC551 - Advanced Digital Design with Verilog and FPGAs  
Fall 2011

Class: Tuesday and Thursday, 4pm - 6pm in PHO 201  
Lab: Section N/A, Tuesdays and Fridays, 2-4pm in PHO 115  
Number of credits: 4, Prerequisites: EC311, EC413

Course Objectives

Content includes the use of a hardware description language (HDL; in particular Verilog) for the specification, synthesis, simulation, and exploration of principles of register transfer level (RTL) designs. Programmable logic, such as field programmable gate array (FPGA) devices, has become a major component of digital design. In this class the students learn how to write HDL models that can be automatically synthesized into integrated circuits using FPGAs. Laboratory and homework exercises include writing HDL models of combinational and sequential circuits, synthesizing models, performing simulation, writing testbench modules, and synthesizing designs to an FPGA by using automatic place and route CAD tools. The course contains lab work and is based on a sequence of Verilog design examples leading to a final group project.

Staff Information

Instructor
Name: Prof. Douglas Densmore  
Office: PHO 335  
Office phone number: 617-358-6238  
E-mail address: dougd@bu.edu (Best way to contact me - Include EC551 in the subject line)  
Office Hours: PHO 335, Wednesdays 6pm-7pm, Fridays 9:30am-10:30am or by appointment

Lab Assistant
Name: Xulei Liu  
E-mail address: liuxulei@bu.edu (Include EC551 in the subject line)  
Office Hours: PHO 115, Tuesdays and Fridays, 2:30pm-3:30pm

Course Resources

Required Textbooks

1. Author: M.D. Ciletti  
   Title: Advanced Digital Design with the Verilog HDL (2nd Edition)  
   ISBN: 0136019285

Optional Textbooks

1. Author: David R. Smith, Paul Franzon  
   Title: Verilog Styles for Synthesis of Digital Systems  
   ISBN: 0201618605
2. Author: Samir Palnitkar  
   Title: Verilog HDL  
   ISBN: 0132599708

Announcements, course material and other useful links

Will be posted on Blackboard (http://blackboard.bu.edu)  
• EC551/Fall 2011

Goals
To provide students with:
• An experience of how to write HDL models that can be automatically synthesized into integrated circuits using programmable hardware such as FPGAs.
• An understanding of how to take a electronic design from concept to register transfer level (RTL) verification and synthesis to final programmable device implementation.
• An experience in writing HDL models of combinational and sequential circuits, synthesizing models, performing simulation, writing test modules, and fitting designs within resource, power, and timing constraints of an FPGA by using automatic place and route CAD software.

Course Outcomes

As an outcome of completing this course, students should be able to:
• Understand advanced topics in digital logic design
• Understand proven design methodologies based on standard CAD tools
• Understand the differences and similarities in hardware and software design
• Understand modern specification methods (HDL)
• Design combinational devices with a full set of CAD tools (skills)
• Understand modeling and verification with hardware description languages
• Understand synthesis with HDLs
• Understand programmable logic devices and FPGAs
• Design state machines, datapath controllers, and assorted CPUs with a full set of CAD tools
• Understand synchronization across clock domains
• Understand timing analysis
• Understand fault simulation and testing

Evaluation

Grading

Midterm - 10%  
Final Exam - 15%  
Final Project - 35%  
Labs (4) - 30%; (5%, 5%, 10%, 10%)  
Five Homework Assignments - 10% (2% each)
Class participation will help your grade if you are on the border of a grade (e.g. B+ to A-). Class participation includes but is not limited to answering questions in class, attending offices hours, helping others when appropriate in the lab, and serving in a leadership role in your project group.

**Homework**

Homework assignments will be posted on the Blackboard website **two weeks ahead of their due dates.** Homework is to be submitted outside of PHO 335 or in class **before** the beginning of the lecture (4:05 sharp) on the date specified. You can discuss your work **in the abstract** with other students in the class, but you **must write-up the solutions on your own.**

**Labs**

Lab descriptions will be posted on the Blackboard website **two weeks ahead of their due dates.** Lab assignments are done in groups of **two students.** You may remain in the same group for the whole semester or change groups with each lab. This is up to you. **Any partner conflicts should be reported EARLY to Prof. Densmore.**

**Exams**

There will be one midterm exam and a final exam. **The midterm will be 10/13 in class. If you are unable to attend this date, you must provide 1 week advance notice along with appropriate documentation.** The final exam is **12/16 from 3-5pm.** Make up final exams will only be given under extreme circumstances.

**Project**

Work as a team of three to four students. **Project presentations will be during the last week of classes (see schedule).** Project presentations will be done in front of all students and should be treated as a professional presentation. More information regarding the projects will be provided closer to the project due date.

**Course Policy**

- Homework/Lab: The homework assignments must be the result of your individual work (HW) or you and your partner (labs).

- You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and to write the solutions of HW/Lab problems by yourself/group. Copying the solution and/or answer from another student is considered cheating. Two identical HWs/Labs with same mistakes are considered cheating. **No extensions on homeworks or labs will be provided. If you will be absent on a day they are due you should make arrangement in advance with Prof. Densmore.**

- Makeup exams: Makeup exams will be provided if the student receives **prior permission** from the instructor. Emergencies will be dealt on a case-by-case basis. Note that oversleeping, being not
ready, or overload due to projects or coursework in other classes are not valid excuses for requesting a makeup exam.

- Exam/Home/Lab Grade discussion: Grade discussion/corrections should be done within one week after the graded exam of homework is distributed. No grade changes will be made after one week, or after the last day of class.

- I and W grades: As per University policy.

- Honor Code: If you are found cheating on HWs, labs, or examinations, you will be brought up on charges before the Student Academic Conduct Committee whose punishment may include suspension from the University without the right to transfer credits for courses taken elsewhere.

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<thead>
<tr>
<th>Lecture #</th>
<th>Date</th>
<th>Topic Description</th>
<th>Labs Out/Due</th>
<th>Hw Out</th>
<th>Hw Due</th>
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<td>9/6 (T)</td>
<td>Introduction to digital logic design flow</td>
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<td>2</td>
<td>9/8 (Th)</td>
<td>Review of combinational logic</td>
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<td>3</td>
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<td>Review of sequential logic part I – FF, FSMs</td>
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<td>Lab1</td>
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