EC772 - VLSI Graduate Design Project  
Spring 2016 – T-TR 4-6 in EPC 204  
Number of credits: 4, Prerequisites: EC 571 and EC551  
(or equivalent knowledge of Verilog)

Course objective
By the end of the course, you should be able to design a digital CMOS chip based on given specifications

Staff Information
Instructor: Allyn Hubbard  
Office address: 329 PHO  
E-mail address: aeh@bu.edu

Office hours: T,Tr 6-7; Wednesday 12-7: There will be skips due to Faculty Council and University Council and some seminars on Wednesday. This is typically 3:15-5:30. In these cases, I will inform everyone in advance, and will be back around 5:30 pm and usually can stay as late as needed. Often I will be nearby (lab, restroom, coffee…) and I will leave a sign on my door unless it is going to be just a few minutes.

Friday 12-1:15 Exception: There will likely be 1-2 times each month that time must be cancelled. I will announce those times as soon as I know what they will be and I will amend this note.

Course Resources

Reference Books:
- Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, E. Brunvand, Pearson  
  Also, Rabaev (text from ec571)

Announcements, course material and other useful links: Will be posted on Blackboard (http://blackboard.bu.edu)

Evaluation
Grading criterion:

• I and W grades: As per University policy.

Preproposal presentation=10% Three Milestones with presentations = 10% Each, Final Presentation = 10%, Final Report = 50%

*Final Report due on ~Wednesday, May 4, 2016. This might change due to graduation-date-related reporting requirements.