Staff Information
Instructor:
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Course objectives
The class covers the theory and practice of digital hardware design. Students will learn to formulate real world tasks using Boolean algebra and FSM theory, and to apply manual and computer-aided techniques to solve the problems. In addition, they will also learn fundamental circuit design and verification skills using Verilog HDL and FPGAs.

Textbooks

Announcements, course material, updated schedule, and other useful links will be posted on Blackboard (http://blackboard.bu.edu).

Goals
To provide students with:
- An understanding of the basic tools of logic design
- An understanding of sound design methodologies
- An experience with hardware implementation and the use of CAD tools

Course Outcomes
As an outcome of completing this course, students should be able to:
- Understand the applications of logic design
- Understand abstraction and hierarchy in digital design
- Understand what components are available for logic design
- Understand the use of Boolean algebra in logic analysis and design
- Understand logic minimization criteria and methods for use in design
- Understand the concept of state in digital systems
- Design combinational digital logic systems given specifications
• Design sequential digital logic systems (finite state machines) given specifications
• Implement logic designs in hardware and with CAD tools
• Discover component availability and data using the Internet or other resources

Homework: Homework assignments will be posted on the Blackboard website. Homeworks are to be submitted before the specified deadline (tentatively on Thursdays). Little to no credit will be given for late homework.

Labs: Lab assignments will be posted on the Blackboard website. “Complete/Incomplete” grades will be assigned by demonstrating the lab individually, setting at a workstation. A “complete” on the due date will constitute a mark of 100. There will be a schedule of “depreciation” of your score until you get it completed.

Exams: The first two exams will be during class time. The third exam will take place during the scheduled final exam timeslot.

Course Policy
• Homework/Lab: The homework and lab assignments must be the result of your individual work. You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and write the solutions of HW/Lab problems by yourself. Copying the solution and/or answer from another student or source is considered cheating.
• Missing exam/Lab: If you have a legitimate reason for missing an exam, or submitting a late lab assignment, please notify me at least a week in advance in order to schedule a make up time.
• Exam/Home/Lab Grade discussion: Grade discussion/corrections should be done within one week after the graded exam or homework is distributed. No grade changes will be made after one week.
• I and W grades: As per University policy.
• Academic integrity:
  o You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. Copying the layout or the code from another student or source is not acceptable.
  o Clearly reference any sources you used in your work: books, Internet, and your collaborators!