Boston University

EC 578 FABRICATION TECHNOLOGY OF INTEGRATED CIRCUITS

Prerequisite: EC 410
Professor: Kleptsyn
Class hours: MW 2-4
Office hours:
Credits: 4
Lab hours:
Maximum number of students 12

Books:
Also recommended:
Richard C. Jaeger. Introduction to Microelectronic Fabrication. 2002
James D. Plummer, Michael D. Deal, Peter B Griffin. Silicon VLSI Technology. 2000
S.K.Ghandhi. VLSI Fabrication principles 1996.

COURSE CONTENTS

1. Silicon properties, single crystals, crystal structures, unit cells, crystallographic planes, Miller indices. Defects and impurities in crystals.
2. Bands, band structure, doping, p- and n-types of semiconductors, band gap levels.
5. Phase diagrams, solid solubility. Diffusion, Fick’s laws, diffusion from a constant source and with a constant amount; interstitial and substitutional diffusion, diffusion coefficient, activation energy. Design of the diffusion process. Ion implantation.
6. Photolithography and masks. Mask design and fabrication.
7. Photoresist deposition, baking, aligning, developing, BOE etching, photoresist removal.
8. BJT. Field effect, MOSFET. BJT and MOSFET design and fabrication steps.
9. Wet etching and reactive ion etching. DRIE.
In a separate lab section students will use their theoretical background to fabricate semiconductor devices and acquire the skills needed to do research on solid state devices.

**PROJECT**

In this course the practical aspects of the fabrication process are the main focus of attention. Theoretical aspects such as modeling of the physical processes and calculations will be given inasmuch as the time permits.

The first and the main goal of this course is to guide students through the practical steps of making an integrated circuit of their own design. As a rule, those steps including measurements and inspection will be supposed to perform manually for more profound understanding of the physical and chemical processes.

The project consists of three main parts:

1. Design. Students will have to design a circuit (e.g. amplifier), transistors, masks and technological process of the fabrication (wafer level).
2. Fabrication. Students will perform all necessary technological steps starting with plain wafer; the wafer containing a few hundred patterned chips should be presented at the end of the course.
3. Inspection will have to be done after each operation. Final wafer inspection may include checking IC parameters on a probe station.

Grading: Homework 25%, Labwork 50%, Final 25%.