In spite of numerous predictions to the contrary, silicon technology is marching along past the 22nm node and on to ever finer dimensions. Innovations at the technology, device, circuit and system levels continue to enable us to scale in spite of what sometimes appear to be insurmountable problems in power, lack of performance, manufacturability, and so on. To a large degree, these innovations are necessary because no substitute technology has been found as yet and, in fact, it does not appear likely that any such technology will become practical this decade. This leaves us with the need to anticipate and predict the near and medium term futures of CMOS for the next handful of technology nodes. This talk will focus on doing just that and will show how an important new constraint on future system scaling is circuit resilience.

Resilience is the ability of circuits to operate in spite of challenges like noise, difficult environmental conditions, aging and manufacturing imperfections. These factors conspire to cause transient or permanent errors that are indistinguishable from traditional “hard” faults typically caused by defects during fabrication. Without significant innovation at the circuit and system levels, the probability of these events can rise quite dramatically. In the area of SRAM, such phenomena have existed for the last three or four technology nodes but significant investments in this area have indeed allowed continued system level scaling with ever larger on-chip memories. As these same phenomena start attacking integrated circuits more pervasively, there is an urgent need for research and development in this area to avert the problems certain to arise with increased defect rates.

To motivate such research, Dr. Nassif will present a roadmap for predicting the resilience of CMOS circuits down to the 12nm node and show examples of how innovations at the circuit and system levels can indeed be used to prolong the life of CMOS and allow for system level operation in spite of frequent device level defects.