

**ENG EC551 – Fall 2009**

Advanced Digital Design with Verilog and FPGA

**Instructor:** Assoc. Prof. Alexander Taubin

(office: PHO335, phone: 31235 e-mail [taubin@bu.edu](mailto:taubin@bu.edu))

**Course web:** [http://courseinfo.bu.edu/courses/09fallengec551\\_a1/](http://courseinfo.bu.edu/courses/09fallengec551_a1/)

**Schedule/classroom:** Tue, Thu 4:00pm-6:00pm /PHO115

Office Hours: Wed from 2:00 to 4:00 p.m.

**Prerequisites Course:** EC311 Introduction to Logic Design of similar course.

**Objectives:**

In recent years, there has been a trend toward using hardware description languages (HDL) for circuit specification. Creating a HDL model has similarity to writing a software program. The compactness and simplicity of HDL models made them preferable to the corresponding flow, state, and logic diagrams. Circuits can be modeled using various abstraction levels. Powerful synthesis methods capable of generating detailed gate level or transistor level schematics using HDL description of the designed architectures were developed and implemented in CAD tools.

This class is an introduction on the use of HDL (Verilog) for design, synthesis and simulation. Programmable logic, such as field programmable gate array (FPGA) devices, has become a major component of digital design.

In this class you will learn how to write HDL models that can be automatically synthesized into integrated circuits such as FPGA.

The course has a lab. and project orientation – students will take a design from concept to register transfer level (RTL) verification and synthesis and then to programmable device implementation.

Laboratory and homework exercises include writing HDL models of combinational and sequential circuits, synthesizing models, performing simulation, and fitting to an FPGA by using automatic place and route.

Recommended background includes EC311 and experience with a high level language such as C or Pascal.

**Tentative outline:**

- *Introduction:* scope of the course, historical background, motivation for using HDL (Verilog), overview of applications: standard logic vs. programmable logic (PLD, FPGA). - 1 week
- *Introduction to HDL:* basic concepts, basic building blocks and design methods to construct synchronous digital systems, basic construction of HDL. Finite state machine design. 2 weeks
- *HDL design examples.* Introduction to *computer-aided design software*. Principles of register transfer level (RTL) (HDL tool: tutorial and exercises)- 1 week

- Use of hardware design languages for expressing, simulating, and synthesizing of designs. – 1 week
- FPGA devices and programming.- 2 week
- Computer-aided *synthesis and optimization*.- 1 weeks
- *Present and future*: current research trends (Asynchronous design using synchronous HDL design tools; Electronic System Level (ESL) design- SystemC and SystemVerilog)- 2 weeks

### **Laboratories:**

- Overview of the Xilinx ISE tools
- Tutorials on Schematic entry and simulation of a half adder and mux/demux
- Design and simulation of a BCD adder, counters. Use of ChipScope.
- Verilog HDL (Hardware description language). Behavior model. Multiplier.
- Design of a FIFO using a behavior representation.
- Design, synthesis, implementation and programming of controllers and datapath.
- Design and implementation of a divider

### **Required Textbook:**

- M.D. Ciletti, *Advanced Digital Design with the Verilog*, Prentice Hall PTR, 2003, ISBN: 0-13-089161-4 (**Required**)

### **Recommended Textbooks:**

- Clive Maxfield, *FPGAs: Instant Access*, Newnes, 2008, ISBN: 9780750689748
- Wayne Wolf, *FPGA-Based System Design*, Prentice Hall PTR, 2004, ISBN: 0-13-142461-0
- Bhasker, J., *A SystemC Primer*, 2<sup>nd</sup> edition, Star Galaxy Publishing, 2004, ISBN 0-9650391-2-9
- S.Sutherland, S.Davidmann and P.Flake. *SystemVerilog for Design*, Kluwer, 2004, ISBN 1-4020-7530-8
- Samir Palnitkar, *Verilog HDL*, 2nd Edition, Prentice Hall PTR, 2003, ISBN: 0130449113
- Bhasker, J., *Verilog HDL Synthesis – A Practical Primer*, Star Galaxy Publishing, Allentown PA
- S. Sutherland and D. Mills, *Verilog and SystemVerilog Gotchas*, Springer, 2007, ISBN: 978-0-387-71714-2

### **Course Grading**

- Midterm examination (20%)
- Homework (10%)
- Laboratory Assignments (30%)
- Final examination or final project (30%)
- Activity, additional points (10%)