

EC413: Computer Organization – Fall, 2009

Basics

Instructor: Prof. Martin Herbordt, PHO 333, x3-9850
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Mission Statement: “Everything from gates and programs!”

Course Description: EC413 is an introduction to the fundamentals and design of computer systems. The starting point is your basic knowledge of logic design and of high-level language programming. Topics covered include computer instruction sets, assembly language programming, arithmetic logic, design of sequential logic with registers and buses, CPU design (data path, control, integrating datapath and control, pipelining), performance evaluation, memory devices, memory systems including caching and virtual memory, and I/O.

Course Style: EC413 has both theoretical and practical aspects (lots of both!).

Prerequisites: EC311, Introduction to Logic Design
Familiarity with Xilinx ISE CAD tools
High-Level Language Programming

Texts: Patterson & Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, 4th Edition, Morgan Kaufmann, 2009
Waldron, *Introduction to RISC Assembly Language Programming*, Addison-Wesley, 1999
(recommended – book is out of print.)
Readings from: Mano and Kime, *Logic and Computer Design Fundamentals*, Prentice Hall, 2001
Selected articles TBD

Course Mechanics

- **Grading:** Exams: 50%
Quizzes: 10%
Homework Assignments: 10%
Labs: 20%
Final Project: 20%
- **Exams:** There will be two mid-term and a final exam. Exams may be open textbook and open notes (TBD), but no calculators are allowed.

- **Quizzes:** There will be six to ten very short and relatively easy quizzes. Their purpose is to ensure that everybody keeps up. Quizzes are closed book and notes. Quizzes begin and end punctually (e.g., beginning precisely at 2:00 ending at 2:05 and 2:10 for 5 and 10 minute quizzes, respectively). There may also be 2-3 or more “attendance” quizzes.
- **Attendance:** *speaking of attendance* Attendance is essential – much of what we cover in this course will be found nowhere else. This semester I will track attendance, I’m not yet sure yet how, and it is not likely to be graded, but will be used to provide feedback.
- **Homework:** There will be 8-10 homework assignments. Usually homework will be due at the beginning of class on the date specified. A few times during the semester, a homework assignment may be due on a Friday. In that case, homeworks must be put under my door by 5PM. Late homework will be penalized 20% for being one business day late and will not be accepted thereafter. You are encouraged to work together to learn the material and to discuss approaches to solving homework problems. However, *you must come up with and write up the solutions on your own.*
- **Labs/Final Project:** There will be 6-8 labs and a major project. Much more about these later! But the rules for collaboration are the same as for homework: *these are all to be done individually.*

Administration

- **Office Hours:** Our office hours are listed above. The best time to catch me otherwise is right after class; the worst time is right before class! On rare occasion I may be unable to keep office hours, so please contact me before traveling a long way to meet me.
- **Email:** You are required to periodically check your email since that is the way many assignments will be distributed. Questions via email are always good. If the question/answer has general interest, I will broadcast it to the class (leaving the questioner anonymous); if the solution is very involved, we may need to go over it in person. Also, please check your email for unexpected occurrences like errors in assignments, cancellations, etc.
- **Course Web Site:** The CourseInfo site is given above. I will use it to post class notes, lab and homework assignments, homework solutions, and other course information.
- **Incompletes:** Incompletes will only be granted in accordance with university policy, which (broadly) requires a major crisis near the end of the semester.
- **Course Notes:** Class notes will be handed out at the beginning of class (sometimes for several classes). You are encouraged to annotate them during class.
- **Academic Honesty:** Please read the university academic honesty policy. If something is not clear, then ask. In particular, plagiarism is regarded as a serious offence and students engaging in this activity will be reported.
- **In Class Distractions:** *Please turn off cell phones and close laptops at the start of class. I find this extremely distracting*
- **Instructor Errors:** Don’t be shy! If you see me make a mistake, please let me know right away. If you are not sure, that’s even better – it might give me a chance to clarify something.
- **Your success** is something a really care about! All job markets are incredibly competitive, but students who succeed here become successful computer engineers (and doctors, managers, etc.).

Wk	Cl	Date	Lecture Topic	HW	Quiz	Text Ref	Labs/Project	Discussion Topic
1	1	3-Sep	Syllabus and administration. What is computer engineering? CE curriculum at BU	hw 1 out		P&H: Ch 1.1-1.7		
2	2	8-Sep	Computer organization overview: simple computer example, instruction execution, machine code to high-level language.	hw 1 due		P&H: B.1-B.4, 3.9		
	3	10-Sep	C language review, emphasizing relationship to underlying HW.		quiz 1	Notes		
3	4	15-Sep	AL: Assembly Language 1	hw 2 out		P&H: B.9-B.10, 2.1-2.10, Notes	Labs 1a,1b due 9/18	Review sequential logic. Go over lab, including facilities & systems
	5	17-Sep	AL: Assembly Language 2			P&H: B.9-B.10, 2.1-2.10, Notes		
4	6	22-Sep	AL: Assembly Language 3 HfA: Review binary & computer arithmetic	hw 2 due hw 3 out		P&H: B.9-B.10, 2.1-2.10, Notes	Lab 2 due 9/25	AL Q&A Go over Lab 2
	7	24-Sep	HfA: Adders, shift-and-add multipliers and dividers			P&H: 3.1-3.2, C.5 Notes		
5	8	29-Sep	HfA: Advanced multipliers, begin floating point	hw 3 due hw 4 out	quiz 2	P&H: 3.3-3.4 Notes	Lab 3 due 10/2 Buses, Adder	HCA Q&A Go over Lab 3
	9	1-Oct	HfA: floating point Datapaths: begin	hw 5 out		P&H: 3.5		
6	10	6-Oct	Datapaths: 4-bit example w/ALU, MUXes, busses, tri-states, ALUs, register files, pipelined datapath	hw 4 due		Notes P&H: C.7-C.8, 4.1-4.3	Lab 4 due 10/9 ALU	HCA Q&A Go over Lab 4
	11	8-Oct	CPU Design: Instruction encoding/decoding. Begin single cycle per instruction CPU	hw 5 due		Notes P&H: 2, 4.4		
7		13-Oct	Columbus Day Holiday					
		12	15-Oct	EXAM 1 (through Class 10, HW5, Lab2)				
8	13	20-Oct	CPU Design: Finish single cycle datapath Control for single cycle CPU		quiz 3	P&H: 4.4, D.1-D.2	Lab 5 due 10/23 Register File	CPU Q&A Go over Lab 5
	14	22-Oct	CPU Design: Multiple cycle per instruction CPU datapath	hw6 out		Notes P&H 3e		
9	15	27-Oct	CPU Design: multicycle control		quiz 4	P&H: D.3-D.6	Lab 6 due 10/30 Datapath	CPU Q&A Go over Lab 6
	16	29-Oct	CPU Design: finish multicycle control Performance evaluation	hw6 due	quiz 5	Notes, P&H 1.8		
10	17	3-Nov	Pipelining: Ideal pipeline, data hazards, forwarding part 1			Notes P&H C.*	Project Out	Pipelining Q&A Go over project
	18	5-Nov	Pipelining: Forwarding part 2, stalls	hw7 out		P&H: 4.5		
11	19	10-Nov	Pipelined CPUs: control hazards Design Automation			P&H: 4.6	Project: design due 11/13	
	20	12-Nov	Design Automation	hw 7 due hw 8 out		P&H: 4.7		
12	21	17-Nov	Memory			P&H: 4.8 M&K: Memory	Project: datapath due 11/20	
	22	19-Nov	Cache:	hw 8 due		P&H: 5.1-5.3 Notes		
13	23	24-Nov	EXAM 2 (through Class 20, HW8, Lab6)			P&H: 5.1-5.3 Notes		
		26-Nov	Thanksgiving Day Holiday		quiz 6	P&H: 5.1-5.3 Notes		
14	24	1-Dec	Cache:		quiz 6	P&H: 5.1-5.3 Notes	Project: controller due 12/1	
	25	3-Dec	Cache:	hw9 out		P&H: 5.1-5.3 Notes		
15	26	8-Dec	OS: Virtual Memory			P&H: 5.4-5.5 Notes	Project: demo and final report due 12/11	
	27	10-Dec		hw9 due				
16		17-Dec	FINAL EXAM -- Thursday, 9-11					