

ENG EC551 Advanced Digital Design with Verilog and FPGA

2008-2009 Catalog Data:

Prereq: ENG EC 311 and ENG EC 413 or consent of instructor. Content includes use of HDL (Verilog) for design, synthesis and simulation, and principles of register transfer level (RTL). Programmable logic, such as field programmable gate array (FPGA) devices, has become a major component of digital design. In this class the students learn how to write HDL models that can be automatically synthesized into integrated circuits such as FPGA. Laboratory and homework exercises include writing HDL models of combinational and sequential circuits, synthesizing models, performing simulation, and fitting to an FPGA by using automatic place and route. The course has lab orientation and is based on a sequence of Verilog design examples. 4 cr.

Status in the Curriculum: Elective

Class/Lab Schedule:

Lecture: 3 hours/week

Laboratory: 1 hours/week

Textbooks and other required materials:

M.D. Ciletti, Advanced Digital Design with the Verilog (Prentice Hall, 2003)

Reference:

Clive Maxfield, *FPGAs: Instant Access*, Newnes, 2008

Wayne Wolf, *FPGA-Based System Design*, Prentice Hall PTR, 2004,

Bhasker, J., *A SystemC Primer*, 2nd edition, Star Galaxy Publishing, 2004

S.Sutherland, S.Davidmann and P.Flake. *SystemVerilog for Design*, Kluwer, 2004

Samir Palnitkar, *Verilog HDL*, 2nd Edition, Prentice Hall PTR, 2003

Bhasker, J., *Verilog HDL Synthesis – A Practical Primer*, Star Galaxy Publishing

S. Sutherland and D. Mills, *Verilog and SystemVerilog* Gotchas, Springer, 2007

Coordinator:

Alexander Taubin, Associate Professor, ECE Department

Prerequisites by topic:

EC311, EC413

Goals:

To provide students with:

- An experience: how to write HDL models that can be automatically synthesized into integrated circuits such as FPGA.
- An understanding how take a design from concept to register transfer level (RTL) verification and synthesis and then to programmable device implementation.
- An experience in writing HDL models of combinational and sequential circuits, synthesizing models, performing simulation, and fitting to an FPGA by using automatic place and route.

Course Outcomes:

As an outcome of completing this course, students should be able to:

- 1) *Understand* the advanced topics of logic design
- 2) *Understand* sound design methodologies based on standard CAD tools
- 3) *Understand* the differences and similarities in hardware and software design
- 4) *Understand* modern specification methods (HDL)
- 5) *Design* combinational devices with a full set of CAD tools (skills)
- 6) *Understand* modeling and verification with hardware description languages
- 7) *Understand* synthesis with HDLs
- 8) *Understand* programmable logic devices and FPGA
- 9) *Design* state machines, datapath controllers, RISC CPU with a full set of CAD tools
- 10) *Understand* synchronization across clock domains
- 11) *Understand* timing analysis
- 12) *Understand* fault simulation and testing

Course Outcomes mapped to Program Outcomes:

Program:	a	b	c	d	e	f	g	h	i	j	k
Course:	1-4	5-9	5-12	9	1-12	1-12	9	1-12	1-12	1-12	1-12
Emphasis:	5	5	5	4	5	3	4	4	5	5	5

1=not at all; 5=a great deal;

Topics in Project Assignments:

Different every year- 2008 topics:

FPGA Pacman;

AES Cryptography Core with Resistance to Differential Power Analysis;

Event Priority Queue for FPGA Based Discrete Molecular Dynamics Simulation;

A Hardware Simulator to Test the Effectiveness of Fault Detection Circuitry within the Advanced Encryption Standard (AES);

FPGA Guitar hero,

Contribution of Course to Meeting the Professional Component:

Engineering topics: 100%

Math & Basic Science: 0%

General Education: 0%

Prepared by: Alexander Taubin

Date: June 2009